Lumped-Element Equivalent Circuit Modeling of Millimeter-Wave HEMT Parasitics Through Full-Wave Electromagnetic Analysis

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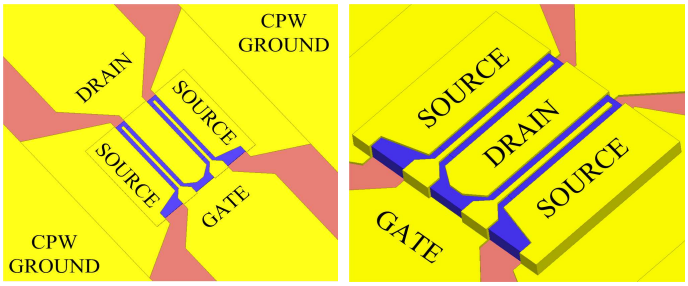
***Abstract*—We present a broadband lumped-element parasitic equivalent circuit to accurately capture the frequency response of electromagnetic interactions inside the structure and surrounding environment of high electron mobility transistors (HEMTs). A new mutual inductance term is included to account for the high-frequency magnetic field coupling between device electrodes. An analytical method is also proposed, for the first time, to extract the gate-to-drain mutual inductance L_{MGD}, which creates an undesirable inductive feedback path from output to input at millimeter-wavelengths. Based on the suggested extrinsic equivalent circuit, we propose a novel multi-step parameter extraction procedure that utilizes direct analytic extraction and linear regression techniques systematically to determine the parasitic component values. The accuracy and robustness of the presented extraction algorithm are established via comprehensive comparisons between electromagnetic simulations, measurements, and frequency responses of the suggested equivalent circuits up to and beyond 300 GHz in the millimeter-wave band. The key parasitic elements that are most detrimental to the microwave performance are identified, and optimized through subsequent circuit analysis. Design guidelines are provided for optimum device layout selection to achieve the highest frequency performance. It is demonstrated through a full-wave simulation based parametric study that around 20% improvement in maximum oscillation frequency is achievable via optimization of device gate finger number and unit finger width.**

***Index Terms*—HEMT, parasitic equivalent circuit model, electromagnetic coupling, layout optimization.**

I. Introduction

AVAILABILITY of accurate device models with wideband accuracy is of utmost importance in realizing radio-frequency (RF) integrated circuits with fewest number of fabrication iterations [1]. For instance, compact transistor models for complex device topologies is critical for the design of state-of-the-art microwave monolithic integrated circuits (MMICs). As the frequency of operation is pushed continuously toward millimeter-wave (mmW) band, the device experiences a serious degradation in its performance. This unavoidable drop in performance arises both from intrinsic device behavior, and external elements comprising parasitic resistance, capacitance, and inductance of device interconnects [2]. Although equivalent circuit modeling has been a workhorse in integrated circuit design, conventional models can not capture the underlying physics of this deterioration in device performance. Perhaps more importantly, the effects of device topology- and material-dependent parasitic couplings associated with electromagnetic (EM) interactions within the device composition and its periphery become as important as those of intrinsic device characteristics at millimeter-wavelengths. In this respect, high-fidelity small-signal device models, which consider intrinsic and extrinsic behavior concurrently, are necessary for effective design of high-performance mmW integrated circuits.



(a) (b)

Fig. 1: Three-dimensional schematics illustrating the structure of a millimeter-wave high electron mobility transistor (HEMT). (a) Top view. (b) Side view.

In accordance with the underlying solid-state and electromagnetic behavior, components of small-signal device models can be partitioned into nonlinear intrinsic elements and linear extrinsic parasitic couplings [3]. Therefore, equivalent circuit extraction procedures begin with identifying bias-independent extrinsic components, followed by subtracting their contributions from the experimental data. Thereafter, bias-dependent intrinsic elements are decided as a function of the externally applied bias voltage. We note here that extrinsic equivalent circuit is bias-independent, and depends essentially on physical geometry of the device, including interconnects, electrode structures, and probing pads. Accurate modeling of extrinsic parasitic elements is thus indispensable, since any erroneous calculation of extrinsic components will result in misinterpretation of intrinsic device performance.

Over the past decade, small-signal equivalent circuits of RF transistors have been primarily studied using measurement-based characterization of fabricated devices [4]-[6]. However, this time-consuming and expensive procedure can only be

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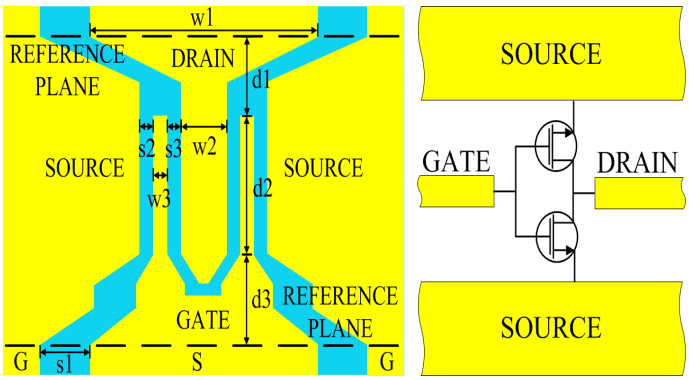


(a) (b)

Fig. 2: Two-finger HEMT layout with coplanar ground-signal-ground (GSG) probe pads. The geometry dimensions are $w_1 = 20$ μm, $w_2 = 4$ μm, $w_3 = 2$ μm, $d_1 = 10$ μm, $d_2 = 28$ μm, $d_3 = 9$ μm, $s_1 = 14$ μm, $s_2 = 2$ μm, and $s_3 = 2$ μm.

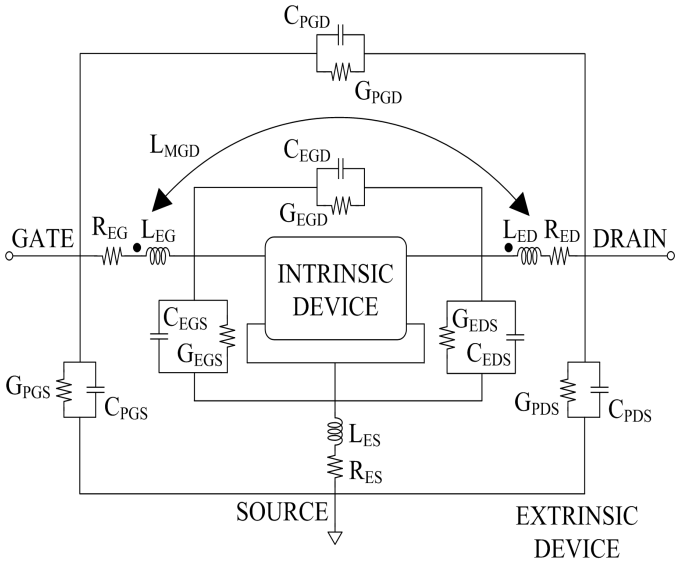


Fig. 3: Lumped-element equivalent circuit model for HEMT describing extrinsic parasitic couplings.

applied to a limited number of device models, typically supplied by the manufacturer. This is due to the need for fabrication and characterization of a separate device when a geometric dimension within the device topology is varied. Another issue related to the equivalent circuit extraction using measured S-parameters is the ill-conditioning of the problem, since there are many more unknowns in the circuit model than the number of equations provided by the experimental data [7]. In order to circumvent this issue, numerical optimization algorithms must be employed, particularly for the extraction of extrinsic parasitic elements. However, the performance of such optimization-driven methods is extremely susceptible to starting parameter values. This is a major shortcoming since they are very likely to converge to inaccurate local minima with physically-meaningless values for the elements in the equivalent circuit. Thus, a new modeling technique which can ensure modeling accuracy and design flexibility at the same time is desperately needed. Here, we develop such a procedure based on full-wave computational models of three-terminal devices.

Commercial full-wave electromagnetic simulators have also been used recently for the analysis of extrinsic parasitic couplings, and lumped-element equivalent circuit extraction [8]. Nevertheless, a numerical optimization tool was employed for the extraction of parasitic components based on simulation data, which still did not provide enough number of equations for precise determination of the extrinsic circuit components. Consequently, a fully analytic parasitic extraction procedure that guarantees physically representative set of parasitic component values is still lacking.

The primary purpose of this paper is to characterize the EM coupling effects that impact the performance of mmW HEMTs. Shown in Fig. 1 is the three-dimensional topology of a millimeter-wave HEMT [9], that is considered in this paper. A conventional lumped-element extrinsic circuit model is employed to predict the frequency response of parasitic couplings in the low-microwave and mmW frequency range. Starting with the conventional circuit model, a new gate-to-drain mutual inductance $L_{\rm MGD}$ is introduced to account for the magnetic flux linkage between gate and drain electrodes. All major electrically- and magnetically-induced power dissipation mechanisms of HEMTs are thus accounted for by the proposed parasitic equivalent circuit model. Based on this improved small-signal circuit model, we present a novel systematic multi-step parameter extraction method to determine the components of the equivalent circuit. The accuracy and robustness of the new methodology are validated through comprehensive comparisons between full-wave EM simulations, measurements, as well as the frequency responses of the proposed test standards up to 325 GHz.

In addition, the impact of EM interactions on microwave performance of HEMTs is evaluated using the proposed equivalent circuit. Subsequently, the device layout is optimized with the objective of improving RF performance. Design guidelines are provided for device topology optimization to accomplish the highest speed attainable from the extrinsic device. The impact of device topology on performance of HEMTs has traditionally been studied through a cumbersome measurement-based approach where many devices with varying geometrical dimensions are fabricated [10]. Subsequently, their measured responses are tabulated and the equivalent circuit parameters are determined through a brute-force curve fitting. On the contrary, the proposed EM simulation-based equivalent circuit extraction strategy is an analytical procedure where individual circuit elements are isolated and accurately determined. As such, the proposed approach also provides the circuit designer with complete freedom in terms of device layout optimization.

In contrast to our recent work [11]-[15], in this paper, we present for the first time a fully analytical method to accurately extract the complete set of parasitic elements, including the proposed gate-to-drain mutual inductance. The improved modeling accuracy of the new model is clearly illustrated through comparison between conventional and the proposed HEMT parasitic equivalent circuits. In addition, a complete set of experimental data is presented to demonstrate the accuracy of the suggested methodology. Furthermore, the

major parasitic elements that are most detrimental to the microwave performance are identified, and readily optimized through subsequent circuit analysis.

The remainder of the paper is organized as follows. In Section II, a detailed description of the structure and geometry of a mmW HEMT with two gate fingers is provided. Following this, a lumped-element parasitic equivalent circuit, intended to achieve broadband modeling accuracy at mmW frequencies, is elaborated. Based on the proposed extrinsic equivalent circuit model, a novel multi-step systematic parameter extraction algorithm is developed. In Section III, the validity of the presented parameter extraction routine is proven via exhaustive comparisons between full-wave EM simulations, measurements, and equivalent circuit frequency responses of the proposed test structures up to 325 GHz. Section IV is devoted to assessment of the adverse impact of EM field interactions on microwave performance of the device under study. The key parasitic components that are most detrimental to the performance are identified through circuit analysis. In Section V, the device periphery is optimized with the purpose of improving speed at millimeter-wavelengths. Finally, concluding remarks are made in Section VI.

II. New Parasitic Equivalent Circuit for HEMTs

In this section, we briefly describe a representative HEMT geometry and the extrinsic electromagnetic mechanisms that impact device parasitics. A three-dimensional HEMT structure illustrated in Figs. 1 and 2 was developed and analyzed in Ansoft High Frequency Structure Simulator (HFSS) [16]. Subsequently, the full-wave simulation data is used in Agilent Advanced Design System (ADS) [17] to determine the extrinsic equivalent circuit elements of HEMT, as shown in Fig. 3.

A. Lumped-Element Equivalent Circuit Model of HEMT External Parasitics

The complete small-signal lumped-element equivalent circuit model of HEMT proposed here is shown in Fig. 3. This improved model includes both extrinsic linear parasitic coupling effects, and intrinsic nonlinear subcircuit as a general nonreciprocal two-port network. As seen, the inter-electrode capacitance-conductance pairs ($C_{\rm EGS}$, $G_{\rm EGS}$), ($C_{\rm EGD}$, $G_{\rm EGD}$), and ($C_{\rm EDS}$, $G_{\rm EDS}$) are connected in parallel with the nonlinear intrinsic device. At high frequencies, these capacitive elements are likely to shunt out the intrinsic transconductance $G_{\rm M}^{\rm INT}$, which provides the gain mechanism of the device. Also included in series with the parallel combination of intrinsic device and inter-electrode capacitance-conductance pairs are the resistance-inductance pairs of gate, drain, and source electrodes, which are denoted as ($R_{\rm EG}$, $L_{\rm EG}$), ($R_{\rm ED}$, $L_{\rm ED}$), and ($R_{\rm ES}$, $L_{\rm ES}$), respectively. These inductances present a high impedance to the incoming and outgoing RF current flow as the frequency increases, and tend to open-circuit the intrinsic device. In addition to these device electrode-related parasitic interactions, the pad-to-pad feedforward capacitance-conductance pairs ($C_{\rm PGS}$, $G_{\rm PGS}$), ($C_{\rm PGD}$, $G_{\rm PGD}$), and ($C_{\rm PDS}$, $G_{\rm PDS}$) are in parallel with the above-mentioned parasitic components. These also create alternative low-impedance RF current flow paths between device terminals. Finally, the mutual inductance $L_{\rm MGD}$ between gate and drain electrodes is incorporated into the proposed circuit model, for the first time, to capture the gate-to-drain magnetic field coupling. The magnetic field coupling between device electrodes originate from their placement in parallel with very close proximity to each other. The consequent inductive crosstalk between gate and drain electrodes creates an undesirable feedback path, in addition to that created by gate-to-drain inter-electrode capacitance of $C_{\rm EGD}$. This may give rise to instabiliy of the device, and deteriorate high frequency performance. As proven in the following, the proposed mutual inductance $L_{\rm MGD}$ is crucial in extending the modeling accuracy beyond 100 GHz, in the millimeter-wave band.

B. Extraction of the External Parasitic Circuit Elements Using Representative Test Structures

The extrinsic parasitic model of the HEMT, shown in Fig. 3, involves 19 circuit elements. As noted before, these circuit elements are often determined in a single step by fitting the measured response of the device to the expected circuit behavior. Although this procedure can also be applied using simulation data, the large number of circuit elements that need to be concurrently determined makes the single-step parameter extraction procedure rather sensitive and unreliable. Here, we develop a multi-step approach for determining the frequency-dependent parasitic elements of the HEMT by strategically dividing the extrinsic circuit model into a number of subcircuits which can be easily fit to experimental or simulation data. Starting with a significantly simplified layout, where the gate and drain electrodes are completely removed from the original device topology as shown in Fig. 4(a), we propose a 6-step process to systematically isolate and identify each parasitic element in the extrinsic circuit. Figure 4 illustrates the 6 proposed layouts of the algorithm. The corresponding lumped-element equivalent circuits for each of the test layouts are given in Fig. 5.

In the first step, gate and drain electrodes are removed, and device contact pads are simulated (or measured) to quantify the degree of electrical coupling and dielectric loss inside the semiconductor layer. The pad layout and the associated equivalent circuit are shown in Figs. 4(a) and 5(a). As seen, only 6 parasitic elements are needed to capture the response of the layout in the first step.

In the second step, device pad and electrode on the drain side are eliminated, and the electrodes of gate terminal are elongated to connect to the gate pad replicated on the drain end. The layout of the THRU1 standard, and the corresponding equivalent circuit are given in Figs. 4(b) and 5(b), respectively. As seen, this symmetric device configuration introduces the gate resistance $R_{\rm EG}$ and inductance $L_{\rm EG}$. In addition, the inter-electrode capacitance-conductance pair of ($C_{\rm EGS}$, $G_{\rm EGS}$) is included to account for the electrical coupling and the dielectric loss between gate and source electrodes.

In the third step, the pad and electrodes of gate terminal are discarded, and the electrode of drain terminal is connected to

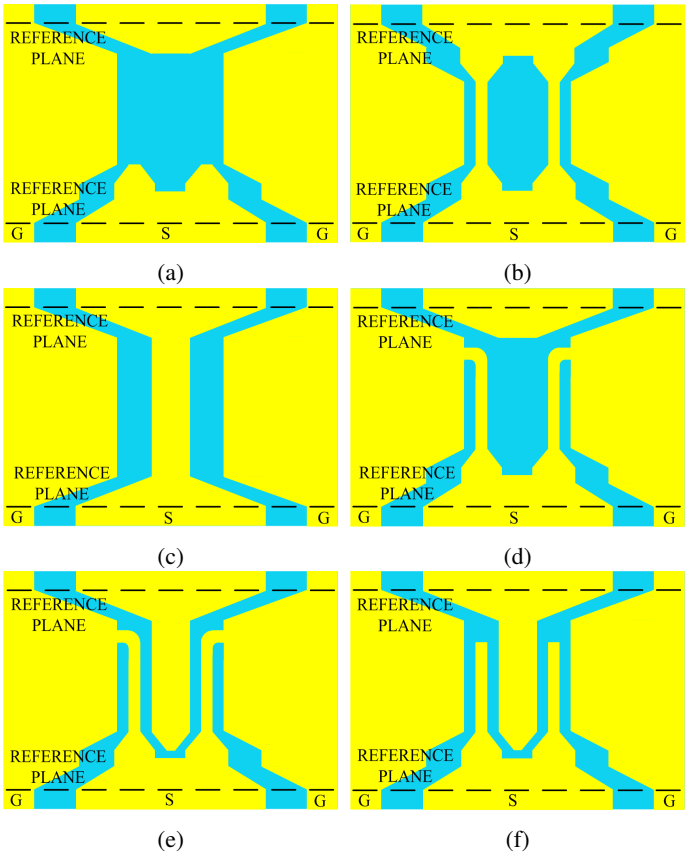


Fig. 4: The proposed on-wafer test standards for HEMT lumped-element parasitic circuit extraction. (a) PADS. (b) THRU1. (c) THRU2. (d) SHORT1. (e) SHORT2. (f) OPEN.

the drain pad replicated on the gate side (THRU2 standard), as shown in Figs. 4(c) and 5(c). The basic aim of investigating this symmetric structure is to capture the variation of resistance R_{ED} and inductance L_{ED} of drain electrode, as the frequency increases steadily into mmW range.

In the fourth step, device electrode on the drain end is removed, and the electrodes of gate terminal are connected to the source electrodes, which are short-circuited to the ground conductor of CPW environment. The layout for this standard (SHORT1), and the corresponding equivalent circuit are illustrated in Figs. 4(d) and 5(d), respectively. The objective of this structure is to isolate the degeneration resistance R_{ES} and inductance L_{ES} of source electrode that degrade the device speed and noise performance severely.

In the fifth step, the electrode of drain terminal is introduced again, and the gate terminal remains short-circuited to the source terminal (SHORT2 standard), as depicted in Figs. 4(e) and 5(e). The main goal of doing so is to capture the impact of L_{MGD} and the associated inductive coupling on overall device impedance.

Finally, in the sixth step, the entire geometry of HEMT is studied to identify the remaining inter-electrode fringe capacitances and conductances. The layout of this OPEN standard, and the related equivalent circuit are given in Figs. 4(f) and 5(f). We note here that the study of OPEN test pattern is similar to the measurement of pinched-off cold HEMT ($V_{\mathrm{GS}} < V_{\mathrm{P}}$, and $V_{\mathrm{DS}} = 0$ V) in conventional HEMT equivalent

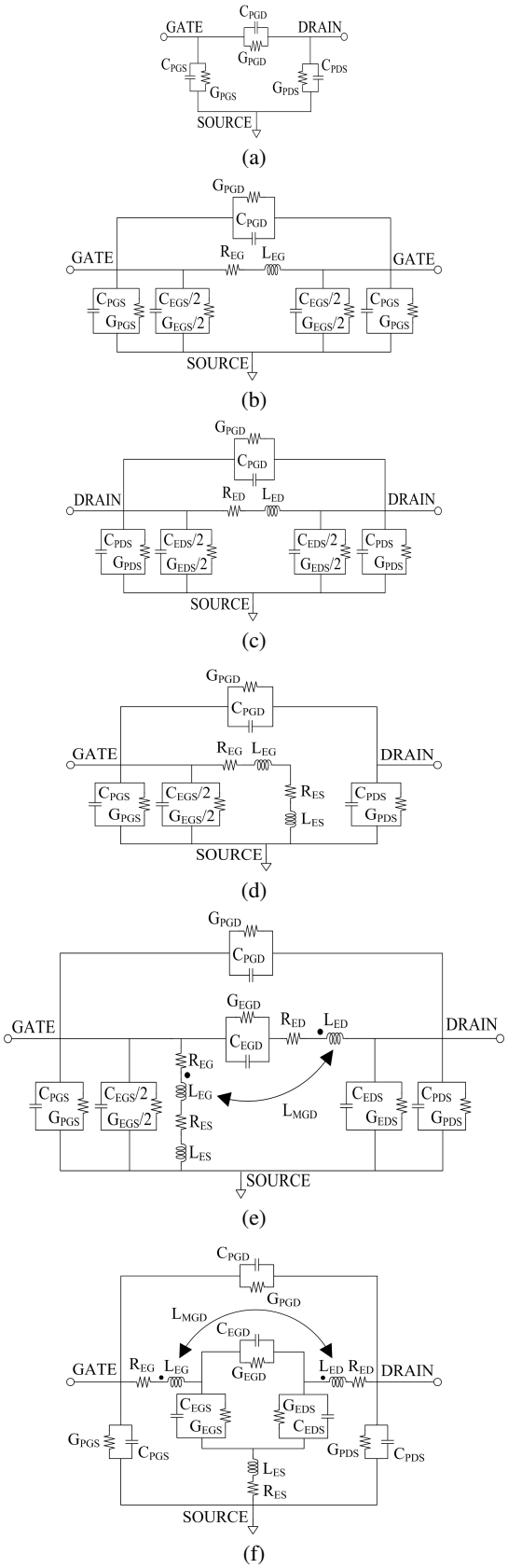


Fig. 5: The proposed lumped-element extrinsic circuit models of HEMT for different steps of parasitic extraction. (a) PADS. (b) THRU1. (c) THRU2. (d) SHORT1. (e) SHORT2. (f) OPEN.

circuit extraction. In pinched-off condition, channel conductivity is suppressed, and device is pushed into a passive state for the determination of extrinsic parasitic network elements [18]. It should also be emphasized that the pad-to-pad capacitances are estimated at lower end of simulated frequency range in Step I of the suggested parameter extraction algorithm. At low microwave frequencies, the reactance associated with the pad inductances is practically short-circuit, and hence has negligible impact on overall frequency response. That is why pad inductances are omitted from the equivalent circuit of PADS standard in Fig. 5(a). Pad inductances are very conveniently extracted from simulation and measurement of THRU1 and THRU2 standards with varying finger width. Those inductances are taken into consideration so as to accurately model the frequency behavior of PADS standard above 100 GHz in the millimeter-wave band.

C. Theoretical Analysis of Extrinsic Parameter Extraction Algorithm

With the above-mentioned strategic choices for six standard layouts, we proceed next to constructing the HEMT equivalent circuit using EM simulations (or measured S-parameters). In Step I, the pad-to-pad capacitances and conductances are determined using the pad layout of Fig. 4(a). We apply a simple linear regression fit to the low-frequency Y-matrix representation of the equivalent circuit shown in Fig. 5(a) to calculate the lumped parasitics using the following matrix relation for the two-port π-network:

$$\left[Y^{\text{PADS}}\right] = \left[\begin{array}{c|c} \begin{array}{c}(G_{\text{PGS}}+j\omega C_{\text{PGS}})\\ +(G_{\text{PGD}}+j\omega C_{\text{PGD}})\end{array} & -(G_{\text{PGD}}+j\omega C_{\text{PGD}}) \\ \hline -(G_{\text{PGD}}+j\omega C_{\text{PGD}}) & \begin{array}{c}(G_{\text{PDS}}+j\omega C_{\text{PDS}})\\ +(G_{\text{PGD}}+j\omega C_{\text{PGD}})\end{array}\end{array}\right]. \tag{1}$$

In Step II, the gate resistance R_{EG} and gate inductance L_{EG} are obtained from the simulation (or measurement) of THRU1 test structure, with the equivalent circuit provided in Fig. 5(b). Initially, the pad-related parasitics extracted in Step I are deembedded from the full-wave simulation results of THRU1 standard using

$$\left[Y^{\text{GATE}}\right] = \left[Y^{\text{THRU1}}\right] - \left[\begin{array}{c|c} \begin{array}{c}(G_{\text{PGS}}+j\omega C_{\text{PGS}})\\ +(G_{\text{PGD}}+j\omega C_{\text{PGD}})\end{array} & -(G_{\text{PGD}}+j\omega C_{\text{PGD}}) \\ \hline -(G_{\text{PGD}}+j\omega C_{\text{PGD}}) & \begin{array}{c}(G_{\text{PGS}}+j\omega C_{\text{PGS}})\\ +(G_{\text{PGD}}+j\omega C_{\text{PGD}})\end{array}\end{array}\right], \tag{2}$$

where

$$\left[Y^{\text{GATE}}\right] = \left[\begin{array}{c|c} \begin{array}{c}(G_{\text{EGS}}+j\omega C_{\text{EGS}})/2\\ +(R_{\text{EG}}+j\omega L_{\text{EG}})^{-1}\end{array} & -(R_{\text{EG}}+j\omega L_{\text{EG}})^{-1} \\ \hline -(R_{\text{EG}}+j\omega L_{\text{EG}})^{-1} & \begin{array}{c}(G_{\text{EGS}}+j\omega C_{\text{EGS}})/2\\ +(R_{\text{EG}}+j\omega L_{\text{EG}})^{-1}\end{array}\end{array}\right] \tag{3}$$

is the admittance matrix representation of the gate electrode-related parasitic couplings. Subsequently, least squares error fit to the elements of $\left[Y^{\text{GATE}}\right]$ can be applied to identify the associated gate-electrode parameters. It is essential to recognize that the lower diagonal entry of the second term on the right hand side of (2) is different from that of $\left[Y^{\text{PADS}}\right]$ expressed in (1). This is because the HEMT layout is not symmetric, that is, gate and drain pads have different geometries, and hence slightly different capacitive coupling with the source pad which is connected to CPW ground.

In Step III, the resistance R_{ED} and inductance L_{ED} of the drain electrode are computed from the THRU2 standard based on the equivalent circuit seen in Fig. 5(c). Similarly to Step II, the simulation or measurement data of THRU2 test pattern is first rearranged to cancel the influence of pad parasitics and obtain auxiliary admittance matrix $\left[Y^{\text{DRAIN}}\right]$, which accounts for the admittance matrix representation of drain electrode-related parasitics. Then, a linear curve fitting is applied to the elements of $\left[Y^{\text{DRAIN}}\right]$ to determine the drain electrode-related parasitic quantities.

In Step IV, source electrode resistance R_{ES} and inductance L_{ES} are found from SHORT1 standard using the equivalent circuit in Fig. 5(d). To do so, simulation (or measurement) results of SHORT1 standard is first corrected for the effects of pad parasitics and gate-to-source inter-electrode capacitance-conductance pair of (C_{EGS}, G_{EGS}) by calculating

$$\left[Y^{\text{SOURCE}}\right] = \left[Y^{\text{SHORT1}}\right] - \left[Y^{\text{PADS}}\right] - \left[\begin{array}{c|c} (G_{\text{EGS}}+j\omega C_{\text{EGS}})/2 & 0 \\ \hline 0 & 0\end{array}\right]. \tag{4}$$

Based on the above, the source resistance R_{ES} and inductance L_{ES} can be computed using

$$R_{\text{ES}} = \text{Re}\left\{\frac{1}{Y_{11}^{\text{SOURCE}}}\right\} - R_{\text{EG}}, \tag{5}$$

$$L_{\text{ES}} = \text{Im}\left\{\frac{1}{Y_{11}^{\text{SOURCE}}}\right\}\Big/\omega - L_{\text{EG}}\ . \tag{6}$$

Next in Step V, the gate-to-drain mutual inductance L_{MGD} is determined using SHORT2 standard, as shown in Fig. 5(e). Initially, the effects of pad-related parasitics, and inter-electrode capacitance-conductance pairs of (C_{EGS}, G_{EGS}) and (C_{EDS}, G_{EDS}) are deembedded from the simulated (or measured) data of SHORT2 layout using

$$\left[Y^{\text{MTL}}\right] = \left[Y^{\text{SHORT2}}\right] - \left[Y^{\text{PADS}}\right] - \left[\begin{array}{c|c} (G_{\text{EGS}}+j\omega C_{\text{EGS}})/2 & 0 \\ \hline 0 & (G_{\text{EDS}}+j\omega C_{\text{EDS}})\end{array}\right]. \tag{7}$$

Afterwards, we transform the auxiliary admittance matrix

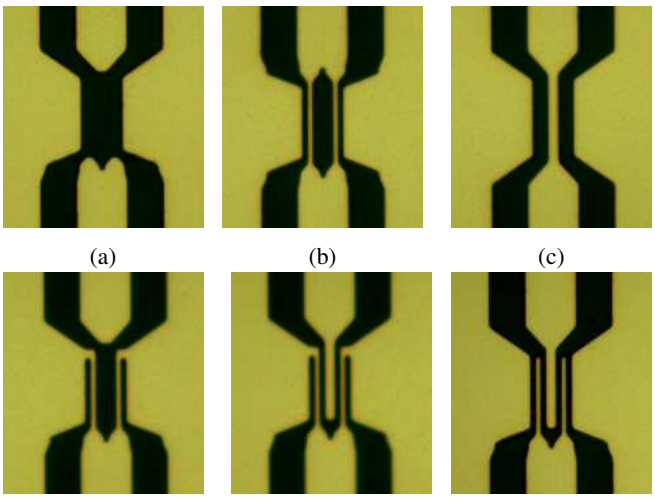


Fig. 6: Micrographs of on-wafer HEMT test standards. (a) PADS. (b) THRU1. (c) THRU2. (d) SHORT1. (e) SHORT2. (f) OPEN.

$[Y^{\text{MTL}}]$ into an impedance matrix $[Z^{\text{MTL}}]$

$$[Z^{\text{MTL}}] = \left[\begin{array}{c|c} \begin{array}{c}(R_{\text{EG}}+R_{\text{ES}})\\ +j\omega(L_{\text{EG}}+L_{\text{ES}})\end{array} & \begin{array}{c}(R_{\text{EG}}+R_{\text{ES}})\\ +j\omega(L_{\text{EG}}+L_{\text{ES}})\\ -j\omega L_{\text{MGD}}\end{array} \\ \hline \begin{array}{c}(R_{\text{EG}}+R_{\text{ES}})\\ +j\omega(L_{\text{EG}}+L_{\text{ES}})\\ -j\omega L_{\text{MGD}}\end{array} & \begin{array}{c}(R_{\text{EG}}+R_{\text{ED}}+R_{\text{ES}})\\ +j\omega(L_{\text{EG}}+L_{\text{ED}})\\ +j\omega(L_{\text{ES}}-2L_{\text{MGD}})\\ +(G_{\text{EGD}}+j\omega C_{\text{EGD}})^{-1}\end{array} \end{array}\right]. \tag{8}$$

By incorporating the above system of equations into a least squares error fitting routine, one can easily extract the gate-to-drain mutual inductance of L_{MGD}.

In the 6$^{\text{th}}$ and final step, the inter-electrode capacitance-conductance pairs of (C_{EGS}, G_{EGS}), (C_{EGD}, G_{EGD}), and (C_{EDS}, G_{EDS}) are estimated using OPEN standard in Fig. 4(f). To do so, the influence of parallel-connected pad-parasitics and series-connected device electrode parasitics are first factored out from the OPEN standard frequency response using

$$[Y^{\text{ELCTR}}] = \left(\left([Y^{\text{OPEN}}] - [Y^{\text{PADS}}]\right)^{-1} - [Z^{\text{SERIES}}]\right)^{-1}, \tag{9}$$

where

$$[Z^{\text{SERIES}}] = \left[\begin{array}{c|c} \begin{array}{c}(R_{\text{EG}}+R_{\text{ES}})\\ +j\omega(L_{\text{EG}}+L_{\text{ES}})\end{array} & \begin{array}{c}R_{\text{ES}}\\ +j\omega(L_{\text{ES}}-L_{\text{MGD}})\end{array} \\ \hline \begin{array}{c}R_{\text{ES}}\\ +j\omega(L_{\text{ES}}-L_{\text{MGD}})\end{array} & \begin{array}{c}(R_{\text{ED}}+R_{\text{ES}})\\ +j\omega(L_{\text{ED}}+L_{\text{ES}})\end{array} \end{array}\right] \tag{10}$$

is the impedance matrix representation of electrode-related

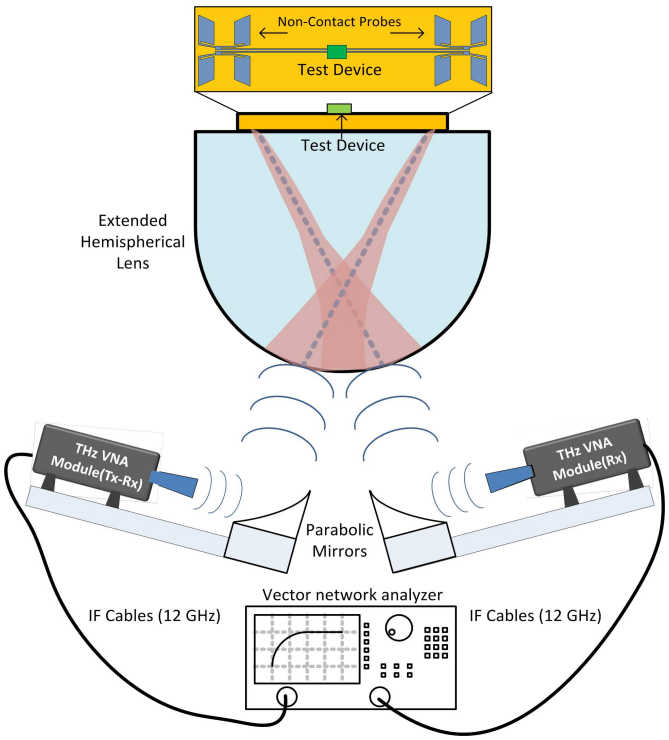


Fig. 7: Block diagram representing the non-contact probe setup.

resistances and inductances, and

$$[Y^{\text{ELCTR}}] = \left[\begin{array}{c|c} \begin{array}{c}(G_{\text{EGS}}+j\omega C_{\text{EGS}})\\ +(G_{\text{EGD}}+j\omega C_{\text{EGD}})\end{array} & -(G_{\text{EGD}}+j\omega C_{\text{EGD}}) \\ \hline -(G_{\text{EGD}}+j\omega C_{\text{EGD}}) & \begin{array}{c}(G_{\text{EDS}}+j\omega C_{\text{EDS}})\\ +(G_{\text{EGD}}+j\omega C_{\text{EGD}})\end{array} \end{array}\right] \tag{11}$$

is the admittance matrix description of inter-electrode capacitances and conductances. Subsequently, a linear regression fit to the elements of $[Y^{\text{ELCTR}}]$ can be utilized to identify the inter-electrode capacitances and conductances.

The estimations of the circuit parameters obtained from (1)-(11) provide excellent starting values for further numerical optimization through least squares error fitting algorithm. To assess the accuracy of the proposed extraction process, the normalized error metric is computed between the full-wave simulated and modeled S-parameters of the device [19]. For the test patterns described in Fig. 4, the average percentage error is less than 10%.

III. Experimental Verification of the Proposed Equivalent Circuit Model

To demonstrate the accuracy of HEMT lumped-element parasitic equivalent circuit extraction procedure developed above, we characterized the HEMT geometry depicted in Fig. 2 over the frequency range of 10-325 GHz. All six proposed test standards were fabricated on a 3-inch GaAs wafer by depositing a single-layer of 0.3 μm thick Au. Figure 6 shows die photographs of the fabricated HEMT test structures. We note that these test standards are passive structures, and do not incorporate any active device. Small-signal measurements

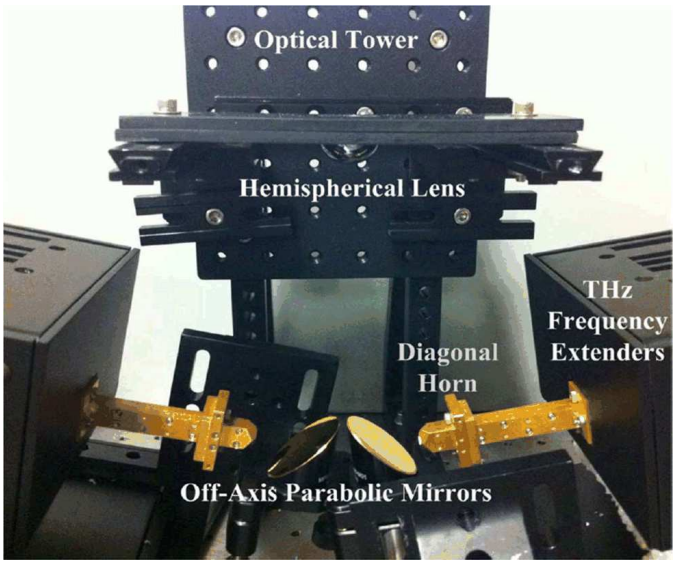
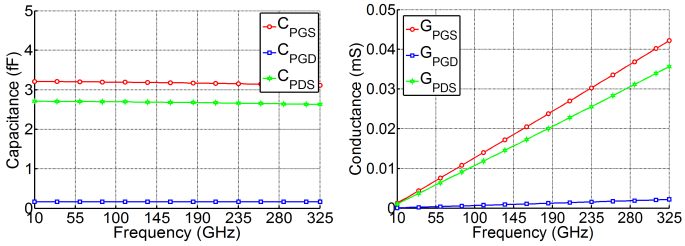


Fig. 8: Non-contact probe setup for S-parameter measurement in millimeter-wave frequency range [20].

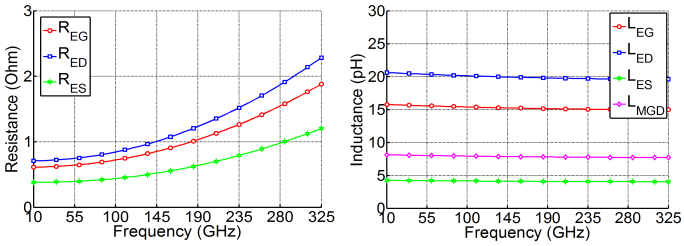
of cold (zero-bias) devices can be used to extract parasitic elements [21]. As such, it is sufficient to consider only the HEMT access topologies and metallization without an active device region to study the effects of external parasitics. In full-wave simulations, the loss tangent of the substrate was set to $\tan\delta = 0.006$ [22], which is in accordance with the low-loss characteristic of GaAs material system. The S-parameters of the fabricated test standards were also measured using a non-contact probe setup [20] over 90-325 GHz band. Since the network analyzer frequency extenders are available only for limited bandwidths, the measurements were taken in three steps over the sub-bands of 90-140, 140-220, and 220-325 GHz, respectively. Operation principle of the non-contact probes is conceptually described in the schematic diagram presented in Fig. 7, where the measured test standard is indicated in the inset. The actual implementation of this quasi-optical system, which is also used in measurement of our test structures, is shown in Fig. 8. Offset-short calibration method was employed for two-port calibration with respect to device reference planes, as illustrated in Fig. 2. On-wafer calibration standards were fabricated on the same substrate as HEMT test patterns shown in Fig. 6. The predicted and measured S-parameters were compared to highlight the extent of agreement between full-wave EM simulations and the experimental data.

The extracted gate, drain, and source inter-pad capacitances and conductances (C_{PGS}, G_{PGS}), (C_{PGD}, G_{PGD}), and (C_{PDS}, G_{PDS}) are shown in Figs. 9(a) and 9(b), respectively. In accordance with the physical layout of the test structure, the feedthrough capacitance of C_{PGD} between gate and drain pads is calculated to be at least 10x smaller than the remaining pad capacitances. As such, C_{PGD} is often omitted from similar extrinsic equivalent circuits reported previously in the literature [23]. In addition, the linearly increasing behavior of the substrate conductances with frequency is in close correlation with the complex-valued dielectric constant relation of $G(\omega)/C(\omega) = \omega\tan\delta$ [24]. The gate, drain, and source electrode resistances and inductances (R_{EG}, L_{EG}), (R_{ED}, L_{ED}), and



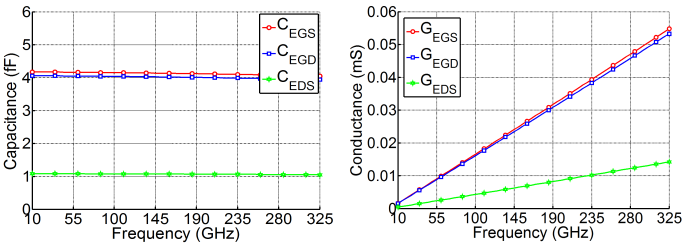
(a) (b)

Fig. 9: Equivalent capacitances and conductances associated with the device pads. (a) C_{PGS}, C_{PGD}, and C_{PDS}. (b) G_{PGS}, G_{PGD}, and G_{PDS}.



(a) (b)

Fig. 10: Device electrode-related equivalent resistance and inductance terms. (a) R_{EG}, R_{ED}, and R_{ES}. (b) L_{EG}, L_{ED}, L_{ES}, and L_{MGD}.

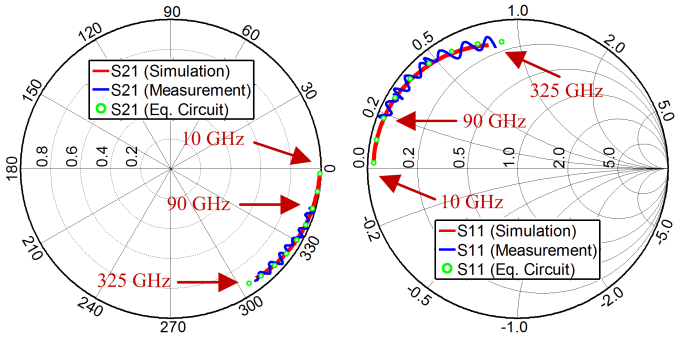


(a) (b)

Fig. 11: Inter-electrode equivalent capacitance and conductance terms. (a) C_{EGS}, C_{EGD}, and C_{EDS}. (b) G_{EGS}, G_{EGD}, and G_{EDS}.

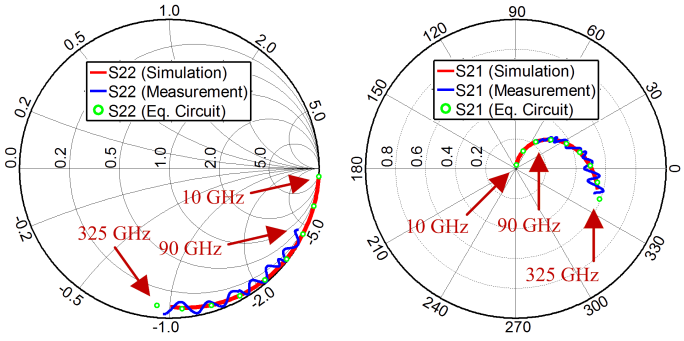
(R_{ES}, L_{ES}) are calculated in Steps II, III, and IV, respectively, and plotted in Figs. 10(a) and 10(b). Compared to almost constant interconnect resistances published previously in the literature [25], the extracted values increase rapidly as the operation frequency varies from low-microwave to millimeter-wave band. This dramatic rise in device metallization resistance is due to the current crowding phenomenon, as described in [26], corresponding to the concentration of current flow to the outer surface of conductor at high frequencies. On the other hand, the gate, drain, and source electrode inductances were not observed to exhibit noticeable change as a function of frequency.

The gate-to-drain mutual inductance of L_{MGD} (computed using simulation of SHORT2 standard) is also given in Fig. 10(b). To the best of authors' knowledge, this is the first time analytical extraction of the gate-to-drain mutual inductance of HEMT transistors has been carried out using experimental data. The limited number of investigations that can be found in the literature are based solely on numerical optimization [27]. This subject has not received substantial attention to date due to the relatively lower frequencies of interest (< 60 GHz) for lumped-element extrinsic equivalent circuits. In this frequency range, the amount of drain-to-gate feedback introduced by this mutual magnetic flux coupling is either marginal or totally



(a) (b)

Fig. 12: Simulated, measured, and circuit model S-parameters for THRU1 and SHORT1 test standards. (a) S_{21}^{THRU1}. (b) S_{11}^{SHORT1}.



(a) (b)

Fig. 13: Simulated, measured, and circuit model S-parameters for SHORT2 and OPEN test patterns. (a) S_{22}^{SHORT2}. (b) S_{21}^{OPEN}.

inconsequential to the device performance. In addition, the impedance associated with the mutual inductance is relatively small at low-microwave frequencies which renders extraction of this component extremely sensitive due to unavoidable measurement uncertainty [28]. However, as the operating frequency is raised into the millimeter-wave regime, the impact of mutual inductive gate-to-drain coupling becomes more pronounced, which necessitates the proposed incorporation of L_{MGD} to the equivalent circuit. The value of the mutual inductance can be determined using the analytical extraction method developed in Section II-C.

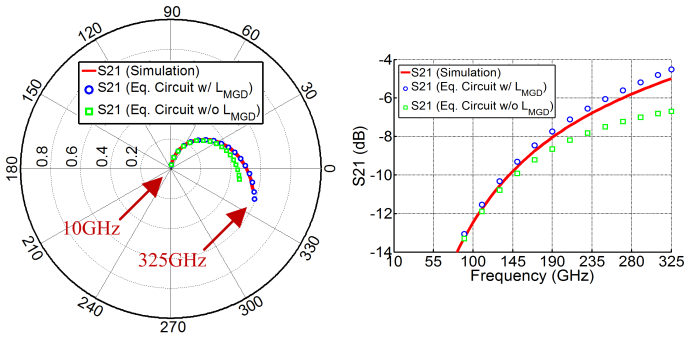
The calculated values of inter-electrode capacitances and conductances of (C_{EGS}, G_{EGS}), (C_{EGD}, G_{EGD}), and (C_{EDS}, G_{EDS}) are given in Figs. 11(a) and 11(b). One important difference between the lumped-element parasitic equivalent circuit proposed here and those presented earlier in the literature is that a significant portion of the previously reported equivalent circuits did not differentiate between the inter-pad and inter-electrode capacitances [29]-[30]. Instead, the entire capacitive coupling between any two device terminals was represented as a single pad-to-pad capacitance. With the aid of this simplifying assumption, it becomes more straightforward to extract the resulting parasitic quantities, but only at the expense of degraded modeling accuracy for the mmW frequencies. In order to maintain the modeling accuracy well into the millimeter-wave frequency band, inter-pad and inter-electrode coupling capacitances need to be treated independently, as is done in this work. Existing studies that differentiate between pad-to-pad and inter-electrode capacitances resort to measurements of devices with varying gate finger widths. Moreover, they rely on linear scalability of inter-electrode capacitances with respect to gate finger width to estimate inter-pad capacitances. [31]-[33]. The total input and output capacitances extracted for different finger widths are extrapolated down to zero finger width to identify inter-pad capacitances. On the contrary, in our approach we developed a completely analytic procedure for the estimation of inter-pad and inter-electrode capacitances without making any assumption related to device geometry or scalability of individual parasitic elements. The proposed analytic parameter extraction routine is therefore more systematic and generic than optimization-based methods published previously in the literature.

In order to validate the accuracy of the presented HEMT parasitic equivalent circuit model, the contact pad- and device electrode-related parasitic elements determined in the first four steps of parameter extraction procedure are substituted into the equivalent circuits of THRU1 and SHORT1 standards given in Figs. 5(b) and 5(d), respectively. Figures 12(a) and 12(b) depict a comparison between the simulated, measured, and circuit model S-parameters for THRU1 and SHORT1 test fixtures in Steps II and IV of the proposed procedure. The S-parameters acquired from full-wave EM simulation show excellent agreement with the measured data over an extremely broad bandwidth. Perhaps more importantly, the simulated S-parameters of the proposed equivalent circuits given in Figs. 5(b) and 5(d) can very accurately reproduce the frequency response of the parasitic couplings over the entire millimeter-wave band.

The ripples observed in Fig. 12 are due to calibration residuals of the non-contact probing setup [20]. Nevertheless, we note that the measured ripple is well below 0.5 dB (at the high-end of the measurement range) for a highly-reflecting load, and does not show any suck-outs or resonance behavior, closely following the simulation results. This effect is also quite repeatable for different devices at different frequencies as shown in this paper as well as in [20], indicating the effectiveness of the measurement setup and calibration methodology.

To further establish the validity of our new methodology, the complete the set of parasitic coupling effects are estimated by executing the six steps of the suggested parasitic extraction algorithm. Following this, the extracted element values are substituted into the equivalent circuits of SHORT2 and OPEN test structures sketched in Figs. 5(e) and 5(f). As recognized from Figs. 13(a) and 13(b), the simulated, measured, and equivalent circuit S-parameters for the two test standards in Steps V and VI of parameter extraction are again in excellent agreement.

The representative comparisons given in Figs. 12(a)-12(b) and 13(a)-13(b) demonstrate the accuracy of the full-wave EM simulations in predicting the measured S-parameters over an extremely broad bandwidth. More importantly, the S-parameters obtained from the equivalent circuit simulation can very accurately track the behavior of EM interactions over the entire mmW band. As seen in Fig. 13(b), transmission coefficient S_{21}^{OPEN} of the OPEN standard increases from virtual open-circuit at low microwave frequencies toward full-transmission



(a) (b)

Fig. 14: Comparison of simulated and modeled transmission coefficient S_{21}^{OPEN} for OPEN test structure illustrating the impact of gate-to-drain mutual inductance L_{MGD}. (a) S_{21}^{OPEN} on polar plot. (b) Logarithmic magnitude of S_{21}^{OPEN}.

in the millimeter-wave region. This steadily-decreasing insertion loss is explained by the fact that the gate-to-drain inter-electrode capacitance C_{EGD} provides an RF current flow path with continuously decreasing capacitive reactance. This example clearly illustrates the dramatic frequency-dependence of parasitic couplings over the microwave to millimeter-wave regime.

It is also worth to emphasize that the transition from capacitive RF current transport at low microwave region to inductive current transport at millimeter-wave frequencies is captured accurately with the aid of gate-to-drain mutual inductance component L_{MGD}. This effect is clearly demonstrated in Figs. 14(a) and 14(b), where the inclusion of L_{MGD} in the equivalent circuit improves its validity region well beyond 100 GHz. Therefore, it is necessary to incorporate gate-to-drain mutual magnetic flux linkage as a separate circuit element into the parasitic equivalent circuit of HEMT to maintain the modeling accuracy at millimeter-wavelengths. This new addition of the gate-to-drain mutual inductance is a key contribution that distinguishes our work from previously reported studies on HEMT parasitic model extraction.

In order to further demonstrate the utility of the proposed methodology, a traditional brute-force optimization algorithm was also employed to estimate equivalent circuit parameters based on the simulation data of the same HEMT layout (i.e., OPEN standard). The extracted circuit elements were $C_{\text{PGS}} = 2.8$ fF, $C_{\text{PGD}} = 0.1$ fF, $C_{\text{PDS}} = 3.2$ fF, $C_{\text{EGS}} = 4.6$ fF, $C_{\text{EGD}} = 4.4$ fF, $C_{\text{EDS}} = 0.5$ fF, $L_{\text{EG}} = 19.8$ pH, $L_{\text{ED}} = 24.3$ pH, $L_{\text{ES}} = 2.1$ pH, $L_{\text{ES}} = 4.9$ pH, $R_{\text{EG}} = 1.2\ \Omega$, $R_{\text{ED}} = 1.5\ \Omega$, and $R_{\text{ES}} = 0.7\ \Omega$ at 325 GHz. As seen, the brute-force optimization-based values, especially the resistances and inductances, deviate substantially from those calculated using our 6-step simulation-based procedure (see Figs. 9-11). It is also important to underline that achieving close agreement between the frequency responses of equivalent circuit and actual device may not necessarily mean that the calculated component values are physically representative. That is, the proposed extrinsic equivalent circuit in Fig. 5(f) contains 19 elements. Any attempt to extract all the elements from a single measurement of a pinched-off cold HEMT will result in an underdetermined system of equations. This problem

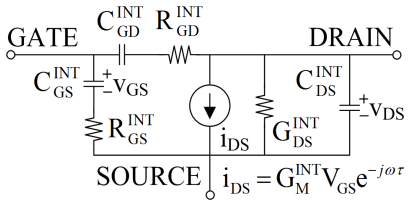


Fig. 15: Intrinsic small-signal equivalent circuit model of HEMT.

is encountered very frequently in the process of extrinsic equivalent circuit extraction, and numerical optimization algorithms are utilized almost exclusively. However, the accuracy of parasitic element values extracted through such numerical optimization routines, as demonstrated in this example, can be quite unreliable due to ill-conditioning of the underlying problem. Consequently, it is necessary to develop a multi-step device modeling strategy so as to precisely determine the parasitic equivalent circuit of millimeter-wave HEMTs, as presented here.

IV. Impact of Parasitic Couplings on High Frequency Performance of HEMTs

The next step in HEMT characterization is to evaluate the impact of parasitic couplings on the high frequency performance of HEMTs. To do so, intrinsic small-signal equivalent circuit parameters of a demonstrated device from the literature is combined with the extrinsic parasitic couplings extracted by using the full-wave simulation-based methodology described in this paper. The intrinsic nonlinear subcircuit of HEMT [34] consists of bias voltage-dependent components shown in Fig. 15. The selected representative device is an AlGaN/GaN HEMT fabricated on a high-resistivity silicon substrate [35]. It has two-fingers, with 90 nm gate-length, and total gate width of $W_{\text{G}} = 2 \times 50\,\mu$m.

The two most important figures of merit (FoMs) for evaluating RF performance of HEMTs are unity current-gain cutoff frequency f_{T} and unity power-gain cutoff frequency f_{MAX}. In order to assess the influence of parasitic couplings on these high frequency performance metrics, the measurement-based intrinsic equivalent circuit components specified in [35] are first used to calculate $\left[Y^{\text{INT}}\right]$, which is the admittance matrix representation of the intrinsic device. Next, the admittance matrix formulation of the extrinsic device is obtained by performing the following matrix operation:

$$\left[Y^{\text{EXT}}\right] = \left(\left(\left[Y^{\text{INT}}\right] + \left[Y^{\text{ELCTR}}\right]\right)^{-1} + \left[Z^{\text{SERIES}}\right]\right)^{-1} + \left[Y^{\text{PADS}}\right], \tag{12}$$

where $\left[Y^{\text{PADS}}\right]$, $\left[Z^{\text{SERIES}}\right]$, and $\left[Y^{\text{ELCTR}}\right]$ are admittance and impedance matrix descriptions of parasitic subcircuits, defined in equations (1), (10), and (11), respectively. Thereafter, Y- to H-matrix conversion of $\left[Y^{\text{EXT}}\right] \longrightarrow \left[H^{\text{EXT}}\right]$ is carried out, and the resulting short circuit current gain ($|H_{21}|^2$) and unilateral power gain (G_{U}) of the intrinsic and extrinsic device are plotted in Fig. 16.

Calculated unity current-gain and power-gain cutoff frequencies of the intrinsic device are $f_{\text{T}}^{\text{INT}} = 134$ GHz, and

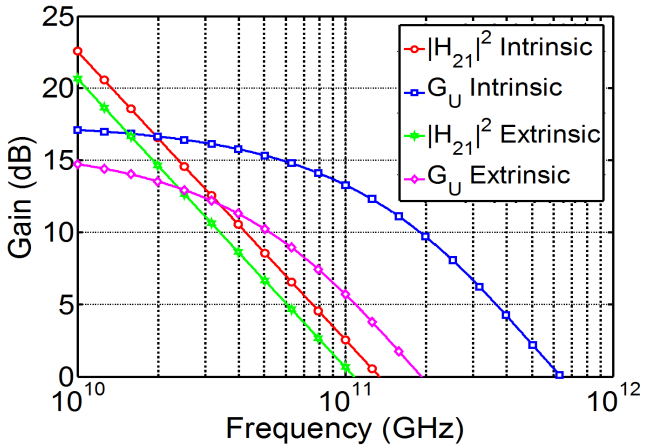


Fig. 16: Simulated current gain $|H_{21}|^2$, and unilateral power gain G_{U} of intrinsic and extrinsic devices.

$f_{\mathrm{MAX}}^{\mathrm{INT}} = 641$ GHz, respectively. For the extrinsic device, the cutoff frequencies are estimated as $f_{\mathrm{T}}^{\mathrm{EXT}} = 108$ GHz, and $f_{\mathrm{MAX}}^{\mathrm{EXT}} = 192$ GHz. The computed extrinsic cutoff frequencies are in excellent agreement with the measured values of $f_{\mathrm{T}}^{\mathrm{EXT}} = 100$ GHz, and $f_{\mathrm{MAX}}^{\mathrm{EXT}} = 206$ GHz, reported in [35]. The amount of degradation in $f_{\mathrm{T}}^{\mathrm{EXT}}$ brought about by the parasitic couplings can be more easily explained by looking at the following approximate expression for $f_{\mathrm{T}}^{\mathrm{EXT}}$

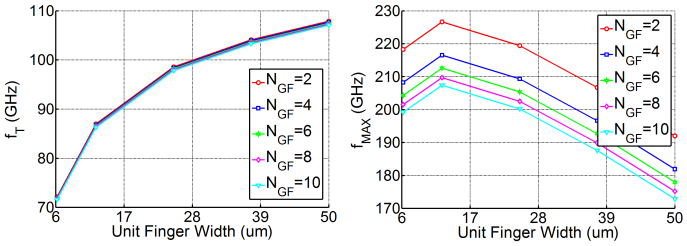
$$\frac{1}{2\pi f_{\mathrm{T}}^{\mathrm{EXT}}} \approx \frac{\left(C_{\mathrm{GS}}^{\mathrm{EXT}} + C_{\mathrm{GD}}^{\mathrm{EXT}}\right)}{G_{\mathrm{M}}^{\mathrm{INT}}} + C_{\mathrm{GD}}^{\mathrm{EXT}}\left(R_{\mathrm{S}}^{\mathrm{EXT}} + R_{\mathrm{D}}^{\mathrm{EXT}}\right) + \left(C_{\mathrm{GS}}^{\mathrm{EXT}} + C_{\mathrm{GD}}^{\mathrm{EXT}}\right)\left(R_{\mathrm{S}}^{\mathrm{EXT}} + R_{\mathrm{D}}^{\mathrm{EXT}}\right)\frac{G_{\mathrm{DS}}^{\mathrm{EXT}}}{G_{\mathrm{M}}^{\mathrm{INT}}}, \tag{13}$$

where $C_{\mathrm{GS}}^{\mathrm{EXT}} = C_{\mathrm{GS}}^{\mathrm{INT}} + C_{\mathrm{PGS}} + C_{\mathrm{EGS}}$, and $C_{\mathrm{GD}}^{\mathrm{EXT}} = C_{\mathrm{GD}}^{\mathrm{INT}} + C_{\mathrm{PGD}} + C_{\mathrm{EGD}}$ are extrinsic gate-to-source and gate-to-drain capacitances [36]. For the device under study, the contributions of second and third terms to the summation in (13) are less than 15%, and 5%, respectively. Accordingly, in order to minimize the impact of EM field couplings on $f_{\mathrm{T}}^{\mathrm{EXT}}$, it is necessary to minimize the ratio of $\left(C_{\mathrm{GS}}^{\mathrm{EXT}} + C_{\mathrm{GD}}^{\mathrm{EXT}}\right) / \left(C_{\mathrm{GS}}^{\mathrm{INT}} + C_{\mathrm{GD}}^{\mathrm{INT}}\right)$, which can be thought of as a measure of the contribution of parasitic gate-to-source and gate-to-drain capacitive couplings to the intrinsic device capacitances. The impact of parasitic couplings on $f_{\mathrm{MAX}}^{\mathrm{EXT}}$ is much more severe than that on $f_{\mathrm{T}}^{\mathrm{EXT}}$, as illustrated in Fig. 16. This is because f_{T} measures the capability of the device to amplify RF current applied to the input. Thus, parasitic resistances play a secondary role in determination of $f_{\mathrm{T}}^{\mathrm{EXT}}$, as also indicated by (13). On the contrary, f_{MAX} quantifies how much power gain is attainable from an amplifier at the frequency of application. The $f_{\mathrm{MAX}}^{\mathrm{EXT}}$ value is therefore subject to ohmic losses related to resistive parasitic elements in the extrinsic equivalent circuit. Consequently, the f_{MAX} is more meaningful figure of merit for deciding the high frequency performance of a device.

The dependence of $f_{\mathrm{MAX}}^{\mathrm{EXT}}$ on parasitic couplings can be better understood by inspecting the following approximate definition for $f_{\mathrm{MAX}}^{\mathrm{EXT}}$

$$f_{\mathrm{MAX}}^{\mathrm{EXT}} \approx \frac{f_{\mathrm{T}}^{\mathrm{EXT}}}{2\sqrt{\left(R_{\mathrm{G}}^{\mathrm{EXT}} + R_{\mathrm{S}}^{\mathrm{EXT}} + R_{\mathrm{GS}}^{\mathrm{INT}}\right)\left(G_{\mathrm{DS}}^{\mathrm{EXT}} + 2\pi f_{\mathrm{T}}^{\mathrm{EXT}} C_{\mathrm{GD}}^{\mathrm{EXT}}\right)}} \tag{14}$$

where $R_{\mathrm{G}}^{\mathrm{EXT}} = R_{\mathrm{EG}}$, and $G_{\mathrm{DS}}^{\mathrm{EXT}} = G_{\mathrm{DS}}^{\mathrm{INT}} + G_{\mathrm{PDS}} + G_{\mathrm{EDS}}$ are extrinsic gate resistance and output conductance [37]. It is immediately apparent from (14) that a significant fraction of the decrease in $f_{\mathrm{MAX}}^{\mathrm{EXT}}$ originates from the access resistances of $R_{\mathrm{G}}^{\mathrm{EXT}}$ and $R_{\mathrm{S}}^{\mathrm{EXT}}$, which are dependent directly on the device topology, i.e., the number of gate fingers N_{GF}, and unit finger width W_{F}.



(a) (b)

Fig. 17: Simulated extrinsic unity current-gain and power-gain cutoff frequencies as a function of unit finger width W_{F}, and number of gate fingers N_{GF}. (a) $f_{\mathrm{T}}^{\mathrm{EXT}}$. (b) $f_{\mathrm{MAX}}^{\mathrm{EXT}}$.

V. Optimum Device Periphery Selection

The final step in HEMT extrinsic equivalent circuit characterization is to demonstrate design optimization capability. In a multifinger transistor structure, the layout of the device is controlled mainly by the number of gate fingers N_{GF}, and unit finger width W_{F}. The total gate periphery W_{G} can be calculated as $W_{\mathrm{G}} = N_{\mathrm{GF}} \times W_{\mathrm{F}}$. It is well known that the elements of admittance matrix $\left[Y^{\mathrm{INT}}\right]$ for the intrinsic small-signal equivalent circuit scale linearly with the total gate periphery W_{G} of the device.

In the course of the following device periphery optimization, the current-gain and power-gain cutoff frequencies of f_{T} and f_{MAX} are studied as a function of the changing device size. The effect of air bridges on parasitic couplings was also taken into consideration for devices having more than two gate fingers. Plotted in Fig. 17(a) is unity current gain cutoff frequency $f_{\mathrm{T}}^{\mathrm{EXT}}$ of extrinsic device with respect to the width per finger W_{F} and gate finger number N_{GF}. As seen in Fig. 17(a), $f_{\mathrm{T}}^{\mathrm{EXT}}$ is approximately independent of the number of gate fingers N_{GF} as long as the width per finger W_{F} is kept constant. This behavior of $f_{\mathrm{T}}^{\mathrm{EXT}}$ as a function of finger number N_{GF} is indeed consistent with the expression in (13). The numerator and the denominator of the first term in the summation scale linearly with the finger number, and hence the ratio stays constant. A similar observation also holds true for the second and third terms in (13). It is further observed that $f_{\mathrm{T}}^{\mathrm{EXT}}$ increases as a function of unit finger width with a decreasing slope, and eventually approaches a steady-state value. As the finger width is increased continuously, the contribution of C_{PGS} to $C_{\mathrm{GS}}^{\mathrm{EXT}}$ becomes progressively more negligible, and $f_{\mathrm{T}}^{\mathrm{EXT}}$ stabilizes around a maximum value. This concave shape

of $f_{\mathrm{T}}^{\mathrm{EXT}}$ curve as a function of finger width W_{F} is also in agreement with the simulation- and measurement-based results published previously in the literature [38]-[39].

The dependence of $f_{\mathrm{MAX}}^{\mathrm{EXT}}$ on the unit finger width W_{F} and the number of gate fingers N_{GF} is plotted in Fig. 17(b). As seen, $f_{\mathrm{MAX}}^{\mathrm{EXT}}$ decreases with respect to increasing width per finger. As already noted, $f_{\mathrm{T}}^{\mathrm{EXT}}$ increases with a decreasing slope, and finally converges to a fixed value, as the unit finger width is raised incessantly. However, the extrinsic elements of $R_{\mathrm{G}}^{\mathrm{EXT}}$ and $C_{\mathrm{GD}}^{\mathrm{EXT}}$ also exhibit a linear increase as a function of unit finger width, and lead to an inevitable degradation in $f_{\mathrm{MAX}}^{\mathrm{EXT}}$ for relatively large values of finger width, as suggested by (14).

Another issue with reduction of width per finger for $f_{\mathrm{MAX}}^{\mathrm{EXT}}$ optimization arises when the finger width gets disproportionately small. For a device with an unnecessarily short finger width, the offset pad-to-pad parasitic capacitance of C_{PGS} dominates the intrinsic gate-to-source and gate-to-drain capacitances of $C_{\mathrm{GS}}^{\mathrm{INT}}$ and $C_{\mathrm{GD}}^{\mathrm{INT}}$. Hence, $f_{\mathrm{T}}^{\mathrm{EXT}}$ drops severely for unreasonably small values of unit finger width, as exemplified in Fig. 17(a). This inevitable drop in $f_{\mathrm{T}}^{\mathrm{EXT}}$ will eventually result in deterioration in $f_{\mathrm{MAX}}^{\mathrm{EXT}}$, as also implied by (14). As a result, the optimum value of finger width for $f_{\mathrm{MAX}}^{\mathrm{EXT}}$ maximization should be selected carefully to manage the tradeoff between short finger width to minimize the gate resistance $R_{\mathrm{G}}^{\mathrm{EXT}}$, and sufficiently large one needed to suppress the adverse effect of offset gate-to-source inter-pad capacitance C_{PGS}. This behavior of $f_{\mathrm{MAX}}^{\mathrm{EXT}}$ as a function of unit finger width is also in close agreement with simulation- and measurement-based studies conducted previously on the subject [40]-[41]. Finally, we note that $f_{\mathrm{MAX}}^{\mathrm{EXT}}$ can be improved by around 20% by choosing a device with two gate fingers and 12.5μm finger width, as seen in Fig. 17(b).

VI. Conclusion

We demonstrated a new lumped-element equivalent circuit model for parasitic couplings of submicron gate-length HEMTs. In addition, we presented a novel equivalent circuit extraction procedure that systematically partitions the HEMT topology, and allows for straightforward determination of parasitic circuit elements. Direct analytic extraction and numerical optimization tools have been utilized in conjunction for the subsequent determination of circuit parameters. An analytical procedure has been offered for the first time to extract the gate-to-drain mutual inductance L_{MGD} using measured data. The accuracy and robustness of the suggested approach have been demonstrated via comprehensive comparisons between simulated, measured, and equivalent circuit frequency responses of the proposed test standards up to 325 GHz. Subsequently, we also demonstrated through a full-wave EM simulation based parametric study that 20% improvement in $f_{\mathrm{MAX}}^{\mathrm{EXT}}$ is realizable through optimization of device gate finger number and unit finger width. Finally, utility of full-wave EM simulation tools as an alternative to fabrication and measurement-based equivalent circuit extraction is verified as a cost-effective solution to device performance optimization in the mmW frequency range.

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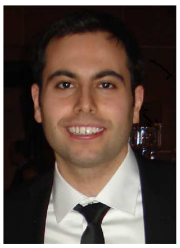

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