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Sub-millimeter-Wave Equivalent Circuit Model for External Parasitics in Double-Finger HEMT Topologies

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Abstract We present a novel distributed equivalent circuit that incorporates a three-way-coupled transmission line to accurately capture the external parasitics of double-finger high electron mobility transistor (HEMT) topologies up to 750 GHz. A six-step systematic parameter extraction procedure is used to determine the equivalent circuit elements for a representative device layout. The accuracy of the proposed approach is validated in the 90-750 GHz band through comparisons between measured data (via non-contact probing) and full-wave simulations, as well as the equivalent circuit response. Subsequently, a semi-distributed active device model is incorporated into the proposed parasitic circuit to demonstrate that the three-way-coupled transmission line model effectively predicts the adverse effect of parasitic components on the sub-mmW performance in an amplifier setting.

Keywords transistors · parasitics · HEMT · distributed circuit modeling · HEMT parasitic extraction

1 Introduction

Advances in heterostructure epitaxy of high-speed semiconductor material systems coupled with novel nanofabrication techniques are enabling new electronic device topologies and functionalities that push viable operation frequencies well into the sub-millimeter-wave bands [1]. Typically, such high-speed devices require extremely short gate lengths, typically on the order of tens of nanometers. As such, the parasitic couplings associated with interconnects and external metalizations constitute a major limiting factor for overall device performance metrics, such as the cutoff frequency. Effects of the external parasitics are well understood for RF and microwave devices, with many existing device modeling approaches that capture the physical capacitances and inductances associated with the contact-lead metals. Nevertheless, the physical dimensions of the device become comparable with the wavelength when the frequency of operation in pushed into the mmW and further into

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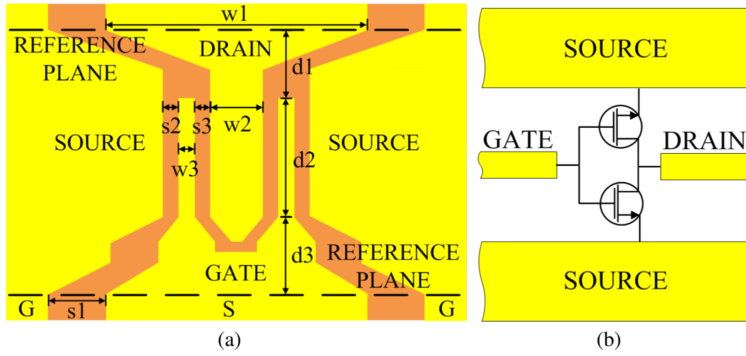


(a) (b)

Fig. 1 Two-finger HEMT layout, and the associated CPW-embedded circuit configuration. Layout dimensions (in μm) are: $w_1 = 10$, $w_2 = 2$, $w_3 = 1$, $d_1 = 6$, $d_2 = 43$, $d_3 = 4$, $s_1 = 7.5$, $s_2 = 1$, and $s_3 = 1$.

the sub-mmW bands. As such, the device physics cannot be accurately captured by simplistic lumped-element circuit models based on quasi-static couplings in the device and contact lead topologies. Although typically the dimensions of the active device regions may still be small compared to the wavelength, the effects of external parasitic couplings must be evaluated properly through full-wave electromagnetic (EM) modeling [2], [3].

In conventional equivalent circuit models of electronic devices, power dissipation and electric/magnetic energy storage inside the device structure are represented by lumped resistive and capacitive/inductive elements [4]. At sub-mmW frequencies, the device inevitably exhibits distributed characteristic along its gate width [5] and a distributed circuit model is necessary for high design fidelity. A large volume of literature exists on the analysis of distributed parasitic coupling effects in field effect transistors (FETs). The commonly-used fully-distributed circuit model provides an accurate description of the wave propagation phenomena within the FET [6], where the gate and drain electrodes are modeled as transmission lines that are coupled with the infinitesimal sections of the intrinsic active device region through EM interactions. Nevertheless, implementation of such fully-distributed models is inconvenient for circuit simulation tools, such as the Advanced Design System (ADS), since such a formulation requires solution of coupled differential equations. Alternatively, a simplified version, known as the semi-distributed model, or sometimes referred to as sliced-model, was proposed in [7]. This model divides the FET device into a finite number of electrically-short active transmission line sections. In essence, the sliced model can be viewed as a discrete approximation to the continuously-distributed circuit model, and more importantly, it can be readily integrated into computer-aided-design (CAD) algorithms of circuit simulators.

Upon constructing a lumped or distributed equivalent circuit model based on device topology and operation frequency, the circuit elements in the model are determined by matching the model's computed response to the experimentally measured data, as exemplified in [8] for a high electron mobility transistor (HEMT). Measured frequency response of pinched-off cold HEMT is conventionally used for determination of parasitic equivalent circuit components [9]-[10]. However, such direct extraction procedures are fundamentally problematic considering the fact that only a limited set of S-parameter measurements are used to determine the all elements in the equivalent circuit. That is, there are many more unknowns than the number of measurements obtained from prototypical device samples. Consequently, device modelers often resort to sophisticated curve-fitting and global-

optimization algorithms [11]-[12] to tackle such under-determined problems and uniquely determine the circuit elements.

However, a major weakness of commonly-used optimization methods is that their final result depends strongly on the initial guesses for the circuit parameter values. Often, the optimization converges to local minima of the cost function, resulting in physically unrealistic solutions. Alternatively, it is also possible to isolate and determine sub-groups of elements in a complex circuit model using a step-by-step, didactic approach where a simpler device topology is used in each step. Since only a small number of circuit elements are determined in each step, and the final circuit mode is built progressively, the optimization problem in each step is much better conditioned and the final results are stable, and guarantee that the overall circuit model captures the physic accurately. As an example, in [4] we demonstrated a six-step approach for determining the lumped-circuit model of a typical double-gate-finger HEMT topology by introducing a mutual inductance term to model the coupling between device electrodes. The new circuit model and the extraction procedure were validated therein with measurements conducted up to 300 GHz.

Thanks to the recent progress in computational electromagnetics, full-wave electromagnetic simulation tools available today are highly accurate and reliable, to the level that their results can replace the measurements that must be conducted using sophisticated and expensive metrology instrumentation. As such, computer-aided empirical models have been studied recently for distributed modeling of FETs. In [13], the extrinsic distributed parasitic network is described in terms of a multi-port *S*-parameter matrix obtained from full-wave EM simulations of the actual device geometry. Although this approach allows the frequency response of distributed parasitic couplings to be completely described via scattering parameters, such a mathematical model does not provide a clear, didactic relation between the device geometry and the resulting frequency characteristics. On the contrary, the elements of the conventional equivalent circuit models can be directly associated with the physical structure of the device, providing much needed insight for device design efforts. Consequently, modeling wave-propagation phenomena through a distributed equivalent circuit network is crucial to provide comprehensive understanding of the relation between device geometry and the related parasitic coupling effects. Furthermore, the knowledge of distributed equivalent circuit model is prerequisite for analysis and prediction of large-signal performance and noise performance-related parameters as well [14].

As noted above, to further improve the circuit model accuracy into sub-mmW frequencies, distributed effects need to be captured in the circuit model. This can be achieved using transmission lines in conjunction with lumped circuit elements in the device models. In [15], we presented initial results of sub-mmW distributed circuit model for a HEMT topology. In this paper, we present the mathematical and procedural details of the six-step parameter extraction method for uniquely determining the equivalent circuit parameters using full-wave simulations of the six standards representing the details of the HEMT access finger topology shown in Fig. 1. The proposed model is based on the extraction procedure, similar to that presented in [4], and the inclusion of transmission line elements is demonstrated here to result in accurate models up to 750 GHz. As described in [4], the equivalent circuit model extraction process is based on full-wave electromagnetic simulations of the six device layouts for each sub-step. Next, we incorporate the external parasitic models with the intrinsic circuit model using a “sliced” model and show that this semi-distributed combined model can predict the key performance parameters of HEMTs, such as the current gain and power gain cutoff frequencies, quite accurately. The paper is organized as follows: In Section 2, we develop a new systematic six-step procedure to extract the proposed distributed equivalent circuit of a double-finger HEMT device using direct analytic extraction in conjunction with

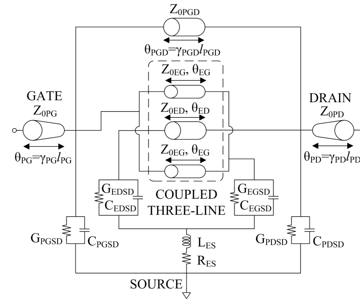


Fig. 2 Proposed distributed equivalent circuit for the commonly-used double-finger HEMT topology.

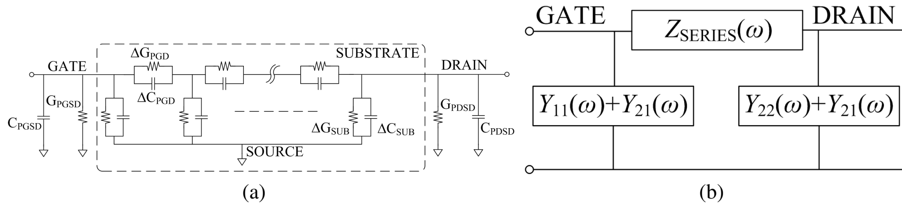


Fig. 3 (a) Distributed equivalent circuit device substrate (b) Standard π-network topology for equivalent circuit extraction.

linear regression. The accuracy of the proposed technique is demonstrated through comparisons of measured results, full-wave simulations, and the performance of the equivalent circuit model's frequency response up to 750 GHz. Subsequently in Section 3, the proposed external parasitic model was incorporated with the active circuit mode of a representative HEMT to illustrate the effectiveness of the proposed approach. Finally in Section 4, we validate the proposed model and the six-step extraction procedure via on-chip characterization between 90-750 GHz using a novel, non-contact probe station.

2 Three-Way Coupled Transmission Line Circuit Model for HEMT External Parasitics

Conventional equivalent circuit models of transistors typically neglect the distributed nature of device electrodes, and thus are not valid at sub-mmW frequencies (see e.g. [4] and the references therein). As noted above, in order to capture wave propagation effects due to the relatively large electrical sizes of device electrodes, distributed circuit elements in form of transmission line segments need to be included in the equivalent circuits for sub-mmW modeling. For the double-finger HEMT topology of Fig. 1 studied here, the coupling between the gate, drain and source electrodes can be incorporated into the device equivalent circuit in form of a three-way coupled transmission line [16], as shown in Fig. 2.

In [4], we demonstrated a lumped-element equivalent circuit by introducing a mutual inductance between the gate and drain fingers of the aforementioned HEMT layout. As in previous conventional models, the displacement and conduction current flowing through the substrate were modeled by parallel inter-pad capacitance-conductance pairs C_{PGD}, G_{PGD}. Although the introduction of mutual inductance between the gate and drain electrodes sig-

nificantly improves the validity frequency range of the circuit model, the lumped-element nature of the model limits its use to frequencies blow 300 GHz.

To account for wave propagation effects through the substrate, here we introduce a distributed substrate network, as inspired from [17] and as depicted in Fig. 3(a). In this distributed equivalent circuit, the substrate-to-ground infinitesimal capacitance-conductance terms of (ΔC_{SUB}, ΔG_{SUB}) are introduced to model the attenuation and propagation characteristics due to the substrate. This distributed substrate network is then integrated into the proposed sub-mmW HEMT equivalent circuit of Fig. 2 as a transmission line having a characteristic impedance $Z_{0\mathrm{PGD}}$ and a propagation constant γ_{PGD}.

The distributed equivalent circuit model of the HEMT topology considered here is based on the standard π-network configuration, as depicted in Fig. 3(b). This π-network topology is based on admittance matrix representation of a reciprocal two-port network, with the series branch replaced by an effective transfer impedance, viz.

$$Z_{\mathrm{SERIES}}(\omega) = \frac{-1}{Y_{21}(\omega)} = R_{21}(\omega) + jX_{21}(\omega) \tag{1}$$

where $R_{21}(\omega)$ and $X_{21}(\omega) = \omega L_{21}(\omega)$ are the effective series transfer resistance and reactance, respectively. Distributed characteristic of gate and drain electrodes at sub-mmW frequencies is directly recognized as a drop in effective series transfer resistance $R_{21}(\omega)$, which can even attain negative values as the operation frequency increases. This nonmonotonic behavior of $R_{21}(\omega)$, as demonstrated in Fig. 17, can not be anticipated by the traditional lumped-element equivalent circuits presented in [4].

As outlined in [4], the equivalent circuit extraction process is based on a 6-step approach, where measurements (or simulation data) from each step is used to progressively determine a few circuit elements at a time. Figure 4 illustrates the six contact leads and finger layouts as the six test structures for the systematic circuit mode extraction utilized here. The distributed parasitic equivalent circuit sub-models corresponding to these test structures are shown in Fig. 5. As seen, the gate and drain contact-pad extensions themselves are also modeled as tapered transmission lines. The contact-pad extensions must be carefully studied and deembedded from the aforementioned test structures through successive applications of Z- and Y-matrix conversions. The characteristic impedance $Z_{\mathrm{C}}(\omega)$ and propagation constant $\gamma(\omega) = \alpha(\omega) + j\beta(\omega)$ of the device contact electrodes are computed by inserting the full-wave simulated and measured S-parameters into [18]

$$Z_{\mathrm{C}}(\omega) = Z_0 \left(\frac{(1+S_{11}+S_{21})(1+S_{11}-S_{21})}{(1-S_{11}-S_{21})(1-S_{11}+S_{21})} \right)^{1/2} \tag{2}$$

$$\gamma(\omega) = \frac{2}{l} \tanh^{-1} \left(\frac{(1+S_{11}-S_{21})(1-S_{11}-S_{21})}{(1-S_{11}+S_{21})(1+S_{11}+S_{21})} \right)^{1/2} \tag{3}$$

where $Z_0 = 50\,\Omega$ is the reference impedance.

Inter-pad capacitance-conductance pairs can be conveniently extracted from the simulation (or measurements) of PADS standard in Step I, using the layout given in Fig. 4(a). After deembedding the contact pads, Y-matrix description of the equivalent circuit in Fig. 3(a) at low frequency is utilized to estimate the lumped pad parasitics according to the following

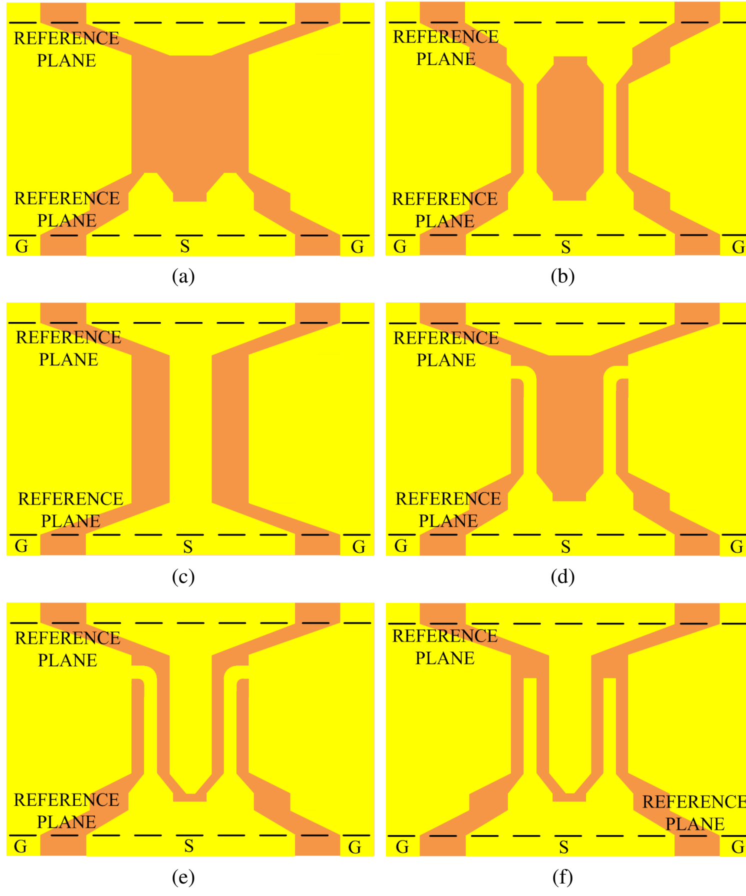


Fig. 4 Layouts of test structures for the proposed distributed model. (a) PADS standard, (b) THRU1 standard, (c) THRU2 standard, (d) SHORT1 standard, (e) SHORT2 standard, (f) OPEN standard.

relations:

$$C_{\mathrm{PGD}} = \frac{-\mathrm{Im}\{Y_{12}\}}{\omega}, \qquad G_{\mathrm{PGD}} = -\mathrm{Re}\{Y_{12}\} \tag{4}$$

$$C_{\mathrm{PGSL}} = \frac{\mathrm{Im}\{Y_{11}+Y_{12}\}}{\omega}, \qquad G_{\mathrm{PGSL}} = \mathrm{Re}\{Y_{11}+Y_{12}\} \tag{5}$$

$$C_{\mathrm{PDSL}} = \frac{\mathrm{Im}\{Y_{22}+Y_{12}\}}{\omega}, \qquad G_{\mathrm{PDSL}} = \mathrm{Re}\{Y_{22}+Y_{12}\} \tag{6}$$

At sub-mmW frequencies, the S-matrix representation of the pad-related parasitic components in Fig. 3(a) can be substituted into (2)-(3) to compute the characteristic impedance $Z_{0\mathrm{PGD}}(\omega)$ and propagation constant $\gamma_{\mathrm{PGD}}(\omega)$ of the distributed substrate network, which is

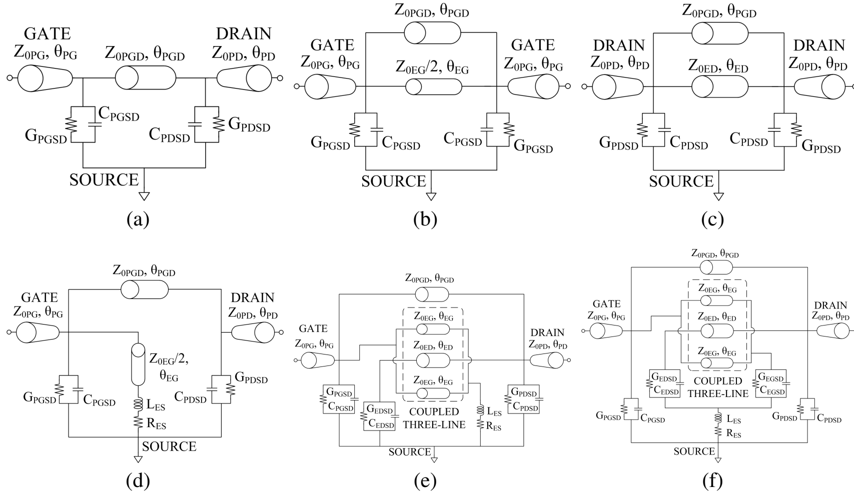


Fig. 5 The proposed distributed extrinsic equivalent circuit representations of the six standards used on parameter extraction: (a) PADS standard, (b) THRU1 standard, (c) THRU2 standard, (d) SHORT1 standard, (e) SHORT2 standard, (f) OPEN standard.

expressed as

$$Z_{0\mathrm{PGD}}(\omega) = \left((G_{\mathrm{PGD}} + j\omega C_{\mathrm{PGD}})\,(G_{\mathrm{SUB}} + j\omega C_{\mathrm{SUB}})\right)^{-1/2} \tag{7}$$

$$\gamma_{\mathrm{PGD}}(\omega) l_{\mathrm{PGD}} = \sqrt{\frac{G_{\mathrm{SUB}} + j\omega C_{\mathrm{SUB}}}{G_{\mathrm{PGD}} + j\omega C_{\mathrm{PGD}}}} \tag{8}$$

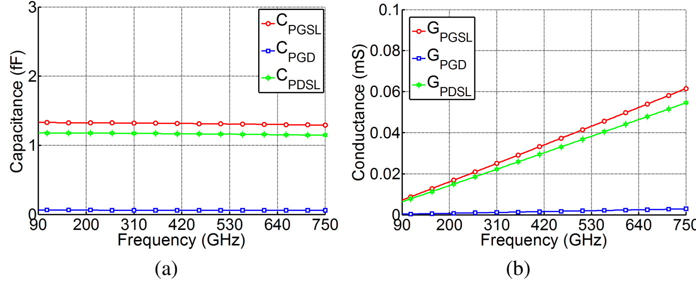
Transmission line parameters of the distributed gate electrodes can be extracted using the THRU1 standard in Step II, with the circuit model shown in Fig. 5(b). First, the contact pads-related parasitic elements obtained from the Step I are factored from the simulation (or measurement) results of the THRU1 structure using

$$\left[Y^{\mathrm{GATE}}\right] = \left[Y^{\mathrm{THRU1}}\right] - \left[Y^{\mathrm{PADS}}\right] \tag{9}$$

where $\left[Y^{\mathrm{PADS}}\right]$ is the admittance matrix representation of distributed substrate network in Fig. 3(a), and $\left[Y^{\mathrm{GATE}}\right]$ is the Y-matrix of the parasitic components related to the gate electrode. Subsequently, the S-matrix transformation of $\left[Y^{\mathrm{GATE}}\right] \longrightarrow \left[S^{\mathrm{GATE}}\right]$ and the resulting S-parameters are plugged into (2)-(3) to compute the characteristic impedance $Z_{0\mathrm{EG}}(\omega)$ and the propagation constant $\gamma_{\mathrm{EG}}(\omega)$ modeling the gate electrodes.

The transmission line parameters of the drain electrode can be similarly calculated from the simulation (or measurements) of the THRU2 standard in Step III, with the circuit model provided in Fig. 5(c). The measured (or simulated) response THRU2 standard is first corrected to eliminate the contribution from the presence pad parasitics, arriving at auxiliary admittance matrix $\left[Y^{\mathrm{DRAIN}}\right]$, for the parasitic couplings related to drain electrode. Subsequently, $\left[Y^{\mathrm{DRAIN}}\right] \longrightarrow \left[S^{\mathrm{DRAIN}}\right]$, and (2)-(3) are again employed to determine the characteristic impedance $Z_{0\mathrm{ED}}(\omega)$ and the propagation constant $\gamma_{\mathrm{ED}}(\omega)$ of the drain electrode.

The resistance R_{ES} and inductance L_{ES} of source electrodes are identified from the simulation (or measurements) of the SHORT1 structure in Step IV, with the circuit model pre-



(a) (b)

Fig. 6 Device pad capacitances and conductances for the HEMT layout with dimensions given in Fig. 1: (a) C_{PGSL}, C_{PGD}, and C_{PDSL}. (b) G_{PGSL}, G_{PGD}, and G_{PDSL}.

sented in Fig. 5(d). To accomplish this, the full-wave data of SHORT1 layout is first rearranged for the contributions of pad parasitics by substracting $\left[Y^{\mathrm{PADS}}\right]$ from $\left[Y^{\mathrm{SHORT1}}\right]$, yielding $\left[Y^{\mathrm{A}}\right] = \left[Y^{\mathrm{SHORT1}}\right] - \left[Y^{\mathrm{PADS}}\right]$. Following this, the auxiliary admittance matrix $\left[Y^{\mathrm{A}}\right]$ is converted into transmission ($ABCD$)-matrix denoted by $\left[T^{\mathrm{A}}\right]$, which is premultiplied by the inverse of transmission matrix representation $\left[T^{\mathrm{GATE}}\right]$ of the gate electrodes to factor out the source electrode transmission matrix

$$\left[T^{\mathrm{SOURCE}}\right] = \left[T^{\mathrm{GATE}}\right]^{-1} \left[T^{\mathrm{A}}\right] \tag{10}$$

Source electrode resistance R_{ES} and inductance L_{ES} can then be calculated using

$$R_{\mathrm{ES}} = \mathrm{Re}\left\{\frac{1}{T_{21}^{\mathrm{SOURCE}}}\right\}, \tag{11}$$

$$L_{\mathrm{ES}} = \mathrm{Im}\left\{\frac{1}{T_{21}^{\mathrm{SOURCE}}}\right\}\Big/\omega \tag{12}$$

The mutual inductance L_{MGD} between gate and drain electrodes is derived from the SHORT2 standard in Step V, with the circuit model presented in Fig. 5(e). Initially, the effects of pad-related parasitics are again subtracted from the response of SHORT2 standard by computing $\left[Y^{\mathrm{MUTUAL}}\right] = \left[Y^{\mathrm{SHORT2}}\right] - \left[Y^{\mathrm{PADS}}\right]$ impedance matrix $\left[Z^{\mathrm{MUTUAL}}\right]$ is obtained. By incorporating the elements of $\left[Z^{\mathrm{MUTUAL}}\right]$ into a numerical optimization algorithm, one can then readily estimate the mutual inductance L_{MGD} between gate and drain electrodes.

Finally, inter-electrode conductance/capacitance pairs ($G_{\mathrm{EDSD}}, C_{\mathrm{EDSD}}$) and ($G_{\mathrm{EGD}}, C_{\mathrm{EGD}}$) are estimated from the simulation of OPEN standard in Step VI, with the circuit model depicted in Fig. 5(f).

For this purpose, the effects of parallel-connected pad-parasitics are first subtracted from the simulation data of OPEN standard using $\left[Y^{\mathrm{ELCTR}}\right] = \left[Y^{\mathrm{OPEN}}\right] - \left[Y^{\mathrm{PADS}}\right]$. Following this, a numerical optimization can be used to obtain the inter-electrode capacitances and conductance values.

The gate, drain, and source inter-pad capacitance-conductance pairs (C_{PGSL}, G_{PGSL}), (C_{PGD}, G_{PGD}), and (C_{PDSL}, G_{PDSL}) are shown in Figs. 6(a) and 6(b), respectively. The extracted value of substrate-to-ground capacitance is $C_{\mathrm{SUB}}{\sim}0.4$ fF. Regarding substrate conductances, the linearly increasing behavior with frequency is in agreement with the dielectric constant relation $G(\omega)/C(\omega) = \omega \tan\delta$ [19]. The characteristic impedance and attenuation constant of gate and drain electrodes are also plotted in Figs. 7(a) and 7(b). In contrast to

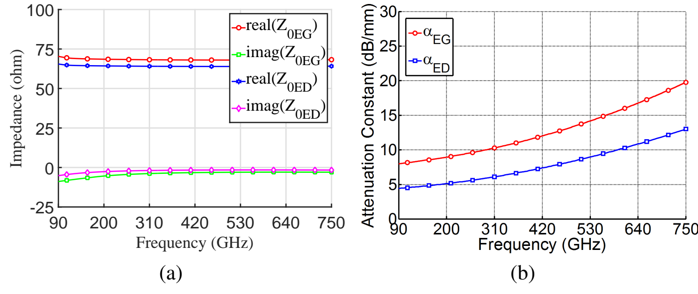


Fig. 7 Characteristic impedance and attenuation constant of gate and drain electrodes. (a) Z_{0EG}, and Z_{0ED}. (b) α_{EG}, and α_{ED}.

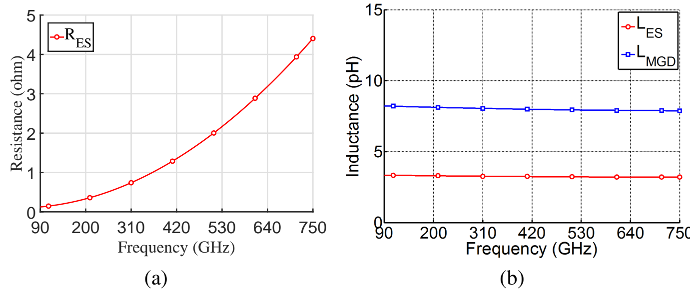


Fig. 8 Resistance and inductance of device electrodes for the HEMT layout of Fig. 1: (a) R_{ES}. (b) L_{ES}, and L_{MGD}.

constant-valued device access metalization resistances reported previously [20], the estimated values of device electrode resistance and consequently the attenuation constant increases significantly as the test frequency moves into to sub-mmW region. Concerning the source electrode resistance and inductance, the extracted values based on full-wave simulations of the SHORT1 layout are given in Figs. 8(a) and 8(b). Also the gate-to-drain mutual inductance L_{MGD}, determined using the SHORT2 structure is given in Fig. 8(b). The extracted value of gate-to-drain inter-electrode capacitance (determined using full-wave simulation of the OPEN standard) is $C_{EGD}\sim$5.7 fF. It is noted that the inter-pad capacitance C_{PGD} and substrate-to-ground capacitance C_{SUB} are more than 10 times lower than the inter-electrode capacitance C_{EGD}. Therefore, coupling through the substrate or between the device pads is observed to have less significant impact on the device frequency response compared to the capacitive coupling between device electrodes.

3 Impact of Parasitic Elements on sub-mmW Performance

To demonstrate the utility of the the external parasitic model for the sub-mmW HEMT topology, we next incorporate the small-signal intrinsic circuit model of a typical device, such as that previously reported in [21]. The intrinsic active sub-circuit of the HEMT is given per unit gate width, and consists of bias voltage-dependent circuit elements, depicted in Fig. 9 . The intrinsic non-linear active device is typically characterized through measurements. Here, we simply incorporated the intrinsic model reported in [21] into the external parasitic

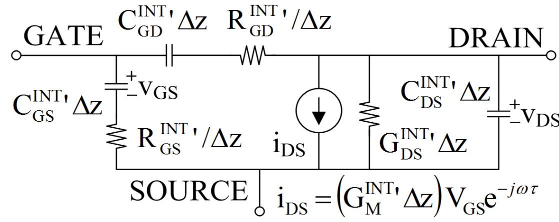


Fig. 9 Intrinsic small-signal active circuit model of the HEMT per unit gate width.

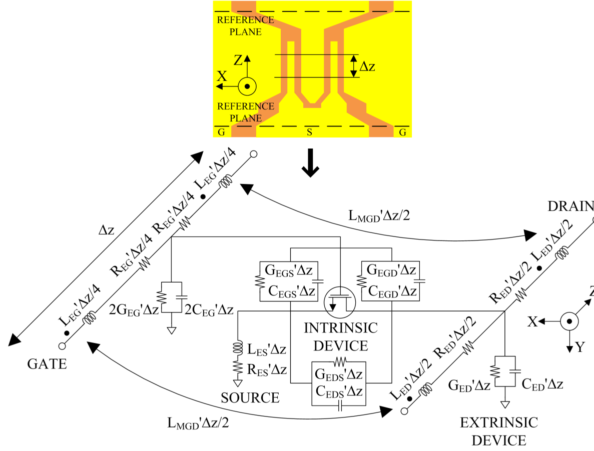


Fig. 10 Extrinsic small-signal equivalent circuit model of HEMT per unit gate width, including parasitic components.

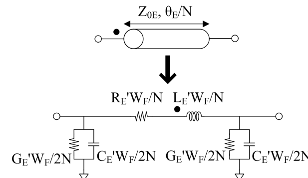


Fig. 11 Low-pass π-network approximation of an electrically-short transmission line section.

small-signal equivalent circuit based on the three-way coupled transmission lines, as shown in Fig. 10. Thereafter, this “incremental” extrinsic equivalent circuit network is multiplied by W_G/N, where W_G is the total gate width of the device, and N is the number of stages that are cascaded to obtain the overall semi-distributed (or *sliced*) model of HEMT, as depicted in Fig. 12.

That is, each such stage is modeled as an intrinsic HEMT with a gate width of W_G/N, and the consecutive stages are connected through lossy coupled transmission line elements to obtain a discrete approximation of the distributed behavior. In this *sliced* HEMT model, the electrically-short gate and drain electrode transmission line sections are approximated by the low-pass π-networks as illustrated in Fig. 11. The unit finger width W_F in Fig. 11 stands for the width of the single gate finger.

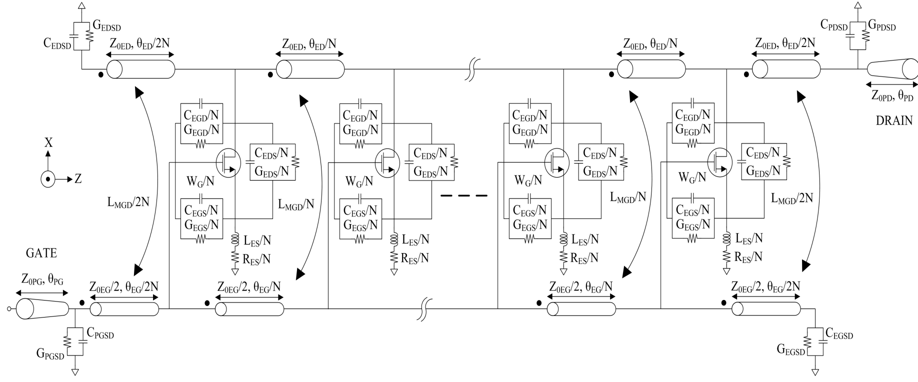


Fig. 12 Semi-distributed (sliced) model of HEMT, including intrinsic nonlinear and extrinsic linear parasitic elements. Transmission line sections are used to represent the low-pass π-network equivalent of electrically-short transmission line elements described in Fig. 11.

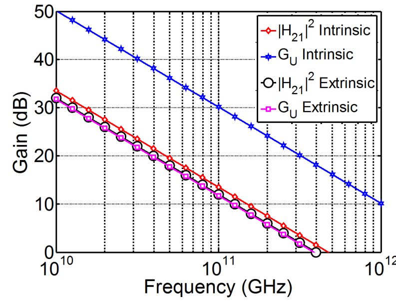


Fig. 13 Current gain $|H_{21}|^2$, and unilateral power gain G_{U} of the intrinsic and extrinsic HEMT model.

The device considered here for high frequency performance analysis is an AlN/GaN/ AlGaN HEMT fabricated on Silicon Carbide [22]. The HEMT has two symmetric gate fingers, each with 20 nm length, and a combined gate width of $W_{\mathrm{G}} = 2 \times 37.5\mu$m. To the distributed nature of external parasitics ans their effects on mmW and sub-mmW device performance the nonlinear intrinsic equivalent circuit parameters from [22] (based on measurements) are integrated into the N=10-stage semi-distributed HEMT equivalent circuit of Fig. 12. Next, a circuit simulator is utilized to obtain the current gain ($|H_{21}|^2$), and the Mason's unilateral power gain (G_{U}) of the intrinsic and extrinsic performance, as presented in Fig. 13.

The computed cutoff frequencies of the intrinsic device are $f_{\mathrm{T}}^{\mathrm{INT}} = 475$ GHz for unity current gain, and $f_{\mathrm{MAX}}^{\mathrm{INT}} = 3220$ GHz for power gain, respectively. The cutoff frequencies of the extrinsic device are calculated as $f_{\mathrm{T}}^{\mathrm{EXT}} = 398$ GHz, and $f_{\mathrm{MAX}}^{\mathrm{EXT}} = 387$ GHz. As seen, the extrinsic cutoff frequencies calculated above using the proposed equivalent circuit are in good agreement with the measured results reported in [22] as $f_{\mathrm{T}}^{\mathrm{EXT}} = 454$ GHz, and $f_{\mathrm{MAX}}^{\mathrm{EXT}} = 444$ GHz. We note here that only a few dimensions of the overall device geometry were specified in [22].

In order to further demonstrate the necessity of distributed-element modeling for sub-mmW HEMTs, the extrinsic cutoff frequencies of the semi-distributed equivalent circuit in Fig. 12 are studied as a function of the number of cascaded stages N. As shown in 14, the extrinsic transition frequency $f_{\mathrm{T}}^{\mathrm{EXT}}$ is almost independent of the number of cascaded

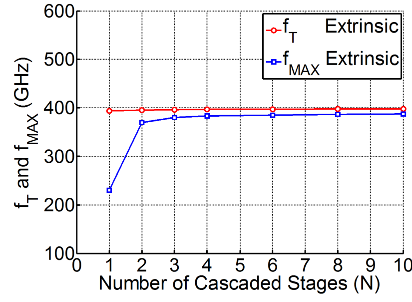


Fig. 14 Extrinsic unity current-gain ($f_{\mathrm{T}}^{\mathrm{EXT}}$), and power-gain ($f_{\mathrm{MAX}}^{\mathrm{EXT}}$) cutoff frequencies as a function of the number of cascaded stages N.

stages N, while the extrinsic maximum oscillation frequency $f_{\mathrm{MAX}}^{\mathrm{EXT}}$ depends strongly on the number of stages in the semi-distributed HEMT equivalent circuit network. The negligible effect of distributed gate resistance on $f_{\mathrm{T}}^{\mathrm{EXT}}$ can be explained by the fact that the device is driven by an ideal current source in $f_{\mathrm{T}}^{\mathrm{EXT}}$ simulation configuration. For the case of $f_{\mathrm{MAX}}^{\mathrm{EXT}}$, the calculated values initially exhibit a steep rise for small number of cascaded stages N, and then converge to a steady-state value for relatively large number of stages. Here, N=1 corresponds to the lumped-element parasitic equivalent circuit and predicts a pessimistic performance expectation because the incoming RF signal is assumed to be attenuated by the entire gate resistance R_{EG} before it gets amplified by the intrinsic transconductance $G_{\mathrm{M}}^{\mathrm{INT}}$. However, in reality, as the incoming RF signal propagates along the gate width, the attenuation by gate resistance R_{EG} and amplification by intrinsic transconductance $G_{\mathrm{M}}^{\mathrm{INT}}$ take place incrementally, as captured by the semi-distributed equivalent circuit model given in Fig. 12. This explains the increase in $f_{\mathrm{MAX}}^{\mathrm{EXT}}$ shown in Fig. 14 with a decreasing slope as a function of the number of cascaded stages N. We note here that overall circuit simulation time depends heavily on the number of stages used in the semi-distributed HEMT model. From the viewpoint of reducing computation time, it is preferable to utilize the least number of stages that can predict the device performance with required level of accuracy within the simulation bandwidth.

4 Experimental Validation of the Accuracy of Full-Wave Simulated Test Standards

To verify the accuracy of the suggested distributed HEMT parasitic circuit extraction technique, the proposed test structures were first simulated over the 10-750 GHz frequency band. Next, test standards were fabricated on a semi-insulating GaAs substrate. The die photographs of the fabricated completely-passive test structures are shown in Fig. 15. Gold evaporation with 0.2 μm thickness was used to metalize the layout and the loss tangent of the substrate was set to 0.009 in full-wave simulations [23].

The S-parameters of the fabricated test patterns were measured using a non-contact probe station, as presented in [24, 25] over the frequency range of 90-750 GHz. The simulation data and the measured S-parameters were studied to illustrate the agreement between full-wave simulations and measurements.

To clearly illustrate the efficacy of the proposed distributed HEMT parasitic model, the responses of THRU2 and SHORT1 standards were characterized in the 90-750GHz band, by combining the contact-pad and device electrode parasitics. As seen in Figs. 16(a) and

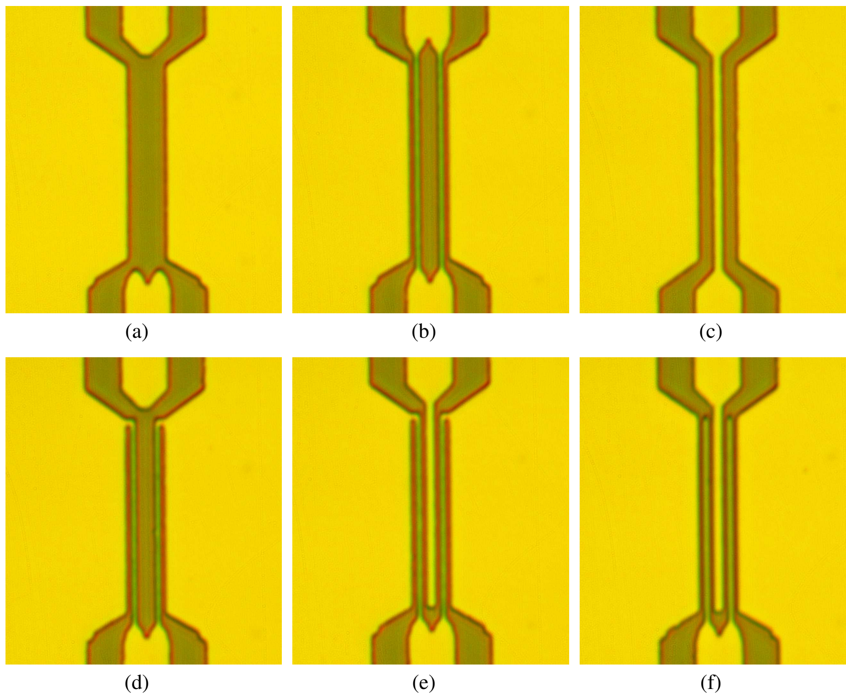


Fig. 15 Micrographs of the fabricated on-wafer test structures for non-contact measurements: (a) PADS standard, (b) THRU1 standard, (c) THRU2 standard, (d) SHORT1 standard, (e) SHORT2 standard, (f) OPEN standard.

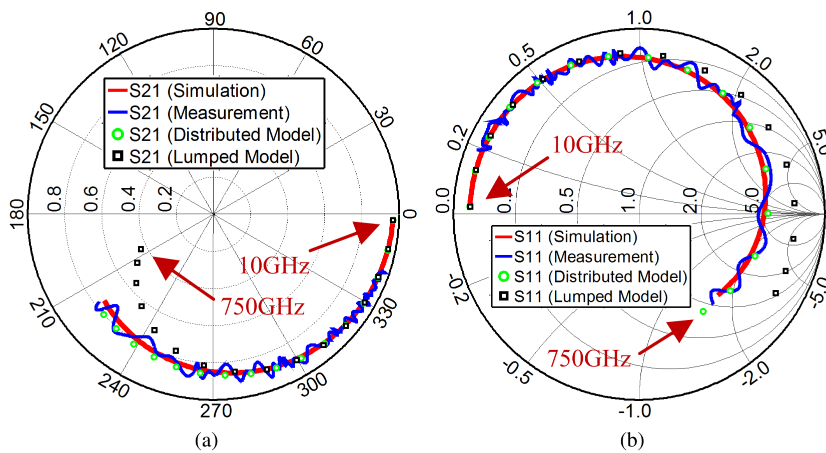


Fig. 16 Measured and simulated *S*-parameters for THRU2 and SHORT1 test standards, as compared with the distributed and lumped circuit model performance: (a) Transmission coefficient S_{21}^{THRU2}, and (b) reflection coefficient S_{11}^{SHORT1}.

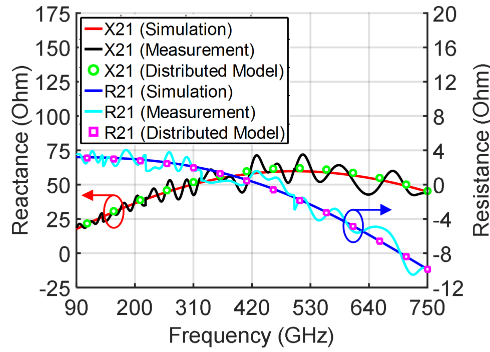


Fig. 17 Effective series transfer impedance $Z_{\mathrm{SERIES}}^{\mathrm{THRU2}}(\omega) = R_{21}(\omega) + jX_{21}(\omega)$ of THRU2 standard in Step III of parasitic model extraction.

16(b) the predicted (full-wave simulations), modeled (circuit response), and measured (non-contact probes) S-parameters for THRU2 and SHORT1 layouts are in excellent agreement in the entire frequency band. In addition, the proposed circuit model captures the S-parameters very accurately over the mmW and sub-mmW bands. On the contrary, the lumped-element circuit model cannot capture the loss and delay characteristics across the device terminals in sub-mmW band. As the electrical length of the device reaches $\sim\lambda_{\mathrm{EFF}}/10$ at $\sim$250 GHz, the lumped-element model starts to deviate from the full-wave simulated behavior. The device geometry used here has a slightly larger gate width, as compared with that presented in [4], as such, the distributed effects of the current device are more pronounced and thus require a more accurate model.

The sharply varying impedance profile with respect to frequency can be better monitored by considering the effective series transfer impedance $Z_{\mathrm{SERIES}}^{\mathrm{THRU2}}(\omega)$ of THRU2 standard, as shown in Fig. 17. For a device with dimensions much smaller than the guided wavelength λ_{EFF}, the conventional lumped-element equivalent circuit approximation (e.g., in [4]) would be valid, and one would observe steadily increasing effective series transfer resistance $R_{21}(\omega)$ and reactance $X_{21}(\omega)$ as a function of frequency. However, as the device dimensions become comparable to a fraction of the effective wavelength at higher frequencies, the rate of increase in $X_{21}(\omega)$ and $R_{21}(\omega)$ gradually drops, and the slope eventually becomes negative for electrically large devices. This nonmonotonic variation of effective series transfer impedance as a function of frequency is direct consequence of the distributed behavior of the device under study, and it is very clearly exemplified by the impedance behavior plotted in Fig. 17.

To further establish the accuracy of the developed distributed parasitic model extraction procedure, the circuit parameters determined throughout the six steps of parasitic extraction are used in the equivalent circuits of SHORT2 and OPEN patterns from Figs. 5(e) and 5(f). Figures 18(a) and 18(b) demonstrate a comparison of simulated, modeled, and measured S-parameters for SHORT2 and OPEN test structures. As seen in Figs. 18(a) and 18(b), the full-wave EM simulation can closely predict the measured S-parameters over a very wide bandwidth. Similarly, the proposed distributed model can also accurately predict the frequency response of EM field interactions over the investigated frequency range, while the lumped-element model fails to account for attenuation, and phase shift across the device terminals in sub-mmW band. The transmission coefficient S_{21}^{OPEN}, plotted in Fig. 18(b), increases steadily because the gate-to-drain inter-electrode capacitance C_{EGD} constitutes an RF current path with capacitive reactance, which decreases as a function of frequency. It

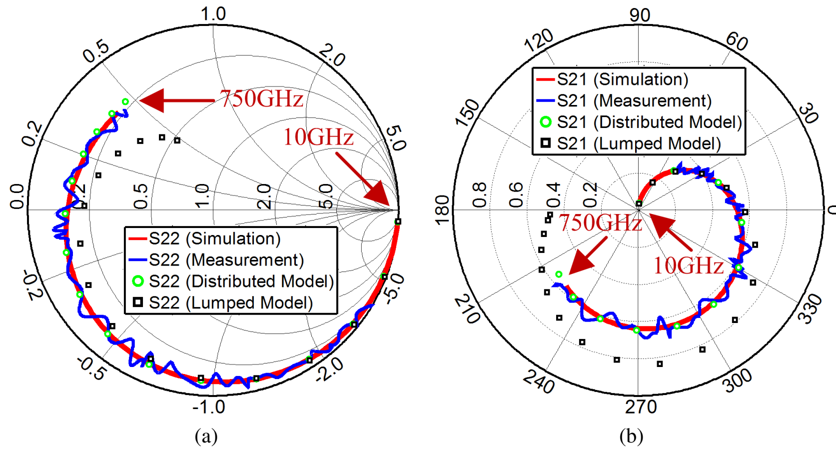


Fig. 18 Simulated, measured, and circuit-model S-parameters for SHORT2 and OPEN test patterns. (a) Reflection coefficient S_{22}^{SHORT2}. (b) Transmission coefficient S_{21}^{OPEN}.

is also important to point out that the transition from capacitive RF current transfer at low frequencies to inductive current transfer in the sub-mmW band is clearly captured, thanks to the inclusion of the gate-to-drain mutual inductance L_{MGD}.

Obviously, the quality of experimentally obtained data directly impacts the accuracy of the extracted parasitic equivalent circuit. In particular for conventional methods, the extracted equivalent circuit parameters are extremely sensitive to measurement errors since the entire parasitic equivalent circuit is extracted from the measurement of a single off-state device. On the contrary, the presented multi-step parameter extraction method is systematic and analytic and it ensures modeling accuracy and robustness in the presence of measurement uncertainty. The proposed iterative algorithm enables us to determine the frequency-dependent parasitic elements of the HEMT by strategically dividing the parasitic circuit model into a number of sub-circuits. The parameters extracted from each simpler device topology in each step are verified with the measured data of the progressively-sophisticated test structures in the forthcoming steps. Only a few equivalent circuit components are estimated in each step, and the overall circuit is constructed systematically. Therefore, the optimization procedure employed in each step is very well-conditioned, and the extracted parameter values are both reliable and physically representative.

5 CONCLUSION

We presented a novel, distributed circuit model that incorporates three-way coupled transmission lines and, as such, accurately captures the electromagnetic parasitic couplings within a typical HEMT structure operating in the sub-mmW band. The equivalent circuit elements can be conveniently determined using the proposed 6-step approach using either measured data or full-wave simulations. Subsequently, the distributed external parasitic circuit model is incorporated with the active intrinsic circuit model of specific device from the literature to demonstrate the predictive performance of the new model. The accuracy of the proposed circuit and the efficacy of the extraction method were extensively demonstrated through

comparisons between simulated, modeled, and measured frequency responses of the test structures for the entire 90-750 GHz.

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